<table>
<thead>
<tr>
<th>Author</th>
<th>ODEH, Charles Ikechukwu.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG/M.ENG/2003/34003</td>
<td></td>
</tr>
<tr>
<td>Title</td>
<td>Multi-Level Pulsewidth Modulation Techniques (PWM) For Multi-Level Inverters.</td>
</tr>
<tr>
<td>Faculty</td>
<td>Engineering</td>
</tr>
<tr>
<td>Department</td>
<td>Electrical Engineering</td>
</tr>
<tr>
<td>Date</td>
<td>January, 2006</td>
</tr>
<tr>
<td>Signature</td>
<td>Ifeanyi Jonas Ezema</td>
</tr>
</tbody>
</table>

Digitally signed by Ifeanyi Jonas Ezema
DN: CN = Ifeanyi Jonas Ezema, C = NG, O = University of Nigeria, OU = University Library
Reason: I have reviewed this document
Date: 2008.12.18 13:19:10 - 12'00'
MULTI-LEVEL PULSEWIDTH MODULATION TECHNIQUES (PWM) FOR MULTI-LEVEL INVERTERS

BY

ODEJI CHARLES IKECHUKWU
PG/M.ENG/2003/34003

DEPARTMENT OF ELECTRICAL ENGINEERING
UNIVERSITY OF NIGERIA, NSUKKA

JANUARY 2006
MULTI-LEVEL PULSE WIDTH MODULATION TECHNIQUES (PWM) FOR MULTI-LEVEL INVERTERS

BY

ODEH, CHARLES IKEDUCHUKWU
PG/ENG/2003/24/005

A thesis submitted in partial fulfilment of the requirements for the award of degree of Masters in Engineering (M.Eng) in Electrical Engineering University of Nigeria, Nsukka January 2006

Author
Odeh, C.I. Date 20/06/06

Supervisor
Dr. M.U. Agba Date 20/06/06

External Examiner
Prof. C.C. Okoro Date 20-06-06

Head of Department
Veh. Engr. Dr. T. C. Madueme Date 20/06/06
MULTILEVEL PULSE WIDTH MODULATION TECHNIQUES
(PWM) FOR MULTILEVEL INVERTERS.
ABSTRACT.

A generalized multilevel inverter topology with self-voltage balancing is presented in this work. It provides a true multilevel structure that can balance each dc voltage level automatically without any assistance from external circuits, thus in principle, providing a complete and true multilevel topology that embraces the existing multilevel inverter configurations. The multilevel voltage source inverter with separate dc sources solves the size- and weight problems of conventional transformer-based multi-pulse inverters and the component-counts problems of multilevel diode-clamp and flying-capacitor inverters.

Various multi-carrier PWM techniques capable of generating multilevel output voltage waveforms are presented. The space Vector Modulation technique, which has superior operational characteristics, is discussed in detail. Operational switching algorithm for M-level inverters is derived and output voltage harmonic spectra for various sampling frequencies are presented.
DEDICATION.

This work is dedicated to GOD ALMIGHTY.
I wish to give my profound gratitude to GOD ALMIGHTY for His infinite creative intelligence, which flows to me copiously, effortlessly and continuously.

I am indebted to Dr. M. U. AGU – my supervisor – for his attention, encouragement and guidance during my consultations with him.

I also give my special thanks to Dr. O. I. OKORO and Dr. S. E. OBE – my lecturers – from whom the materials used in the work were sourced. Also, their counsels provide the driving force for the actualization of this piece of work.
TABLE OF CONTENTS.

CHAPTER ONE: Introduction

CHAPTER TWO: Multilevel converter Topologies

2.1: Generalized multilevel inverter topology with self-voltage balancing. ............................. 4
2.2: Diode-clamp multilevel inverters. .................................................. 11
2.3: Multilevel inverters using flying-capacitors. .............................................. 15
2.4: Multilevel inverters employing cascaded inverters with separate dc sources. .......... 19
2.5: Generalized truth-table representation of multilevel inverter switching states. ........ 25

CHAPTER THREE: Multilevel Pulse Width Modulation (PWM) Techniques

3.1: Sub-harmonic/Multi-carrier PWM strategy. ............................................. 31
3.1.1: Carrier disposition methods. ............................................................... 32
3.1.11: Alternate Phase Opposition disposition (AOPD) modulation. ...................... 32
3.1.12: Phase disposition (PD) modulation. ................................................. 32
3.1.13: Phase Opposition disposition (POD) modulation. .................................. 32
3.1.2: Phase-shift multi-carrier (PS) PWM method ........................................ 32
3.2: Specific Harmonic Elimination technique. .............................................. 38
3.3: Space Vector PWM for M-level converter. ............................................. 38
3.3.1: Vector representation. ................................................................. 39
3.3.2: Coordinate transformation. ............................................................... 45
3.3.3: Detection of the Nearest Tree Vectors (NTV). .................................... 46
3.3.4: Duty cycle computation. ................................................................. 48
3.3.5: Switching state selection. ............................................................... 49
3.3.6: Optimized Space Vector sequences. .................................................. 49
CHAPTER FOUR: Sample calculations

4.1: Unmodulated 3-phase, 2-level inverter

4.2: Unmodulated 3-phase, 3-level inverter

4.3: Unmodulated 3-phase, 4-level inverter

4.4: Unmodulated 3-phase, 5-level inverter

4.5: Space Vector modulated 3-phase, 3-level inverter with line-to-line voltage ($V_{L-L}$) of 1.8$V_{dc}$ and sampling angle ($\alpha_{sL}$) of 60°.

4.6: Space Vector modulated 3-phase, 3-level inverter with line-to-line voltage ($V_{L-L}$) of 1.8$V_{dc}$ and sampling angle ($\alpha_{sL}$) of 30°.

4.7: Space Vector modulated 3-phase, 3-level inverter with line-to-line voltage ($V_{L-L}$) of 1.8$V_{dc}$ and sampling angle ($\alpha_{sL}$) of 20°.

4.8: Space Vector modulated 3-phase, 3-level inverter with line-to-line voltage ($V_{L-L}$) of 1.8$V_{dc}$ and sampling angle ($\alpha_{sL}$) of 10°.

4.9: Specific Harmonic Elimination

CHAPTER FIVE: HARMONIC EVALUATION AND SPECTRA

CHAPTER SIX: DISCUSSIONS AND CONCLUSIONS

REFERENCES
CHAPTER ONE.

INTRODUCTION.

For quite some time, high voltage and/or high power inverter circuits have been realized using output transformers and/or arranging inverters in parallel using the harmonic cancellation technique as the control strategy [1]. These inverters are needed in high power applications such as utility and large motor drive applications. The problem associated with this approach is that these transformers, or harmonic neutralizing magnets produce about 50% of the total system losses. Besides, the inverter control becomes extremely difficult due to dc magnetizing and surge overvoltage problems resulting from saturation of the transformers in transient states. Moreover, these transformers are the most expensive equipment in the system; and constitutes up to 40% of the total system size/weight.

Recently, transformerless multilevel inverters have been developed which drastically reduce the reactive component count and hence inverter weight, and size/bulkiness. This development have been made easy and possible by the rapid development of high power and high speed semiconductor devices (gate turn-off, GTO, thyristors; high voltage insulated gate bipolar thyristor, HVIGBT, and gate commutated thyristors, GCT). The multilevel voltage source inverter's unique structure allows it to reach high voltage without the use of transformers or series-connected synchronized switching devices. The general function of the multilevel inverter is to synthesize a desired output ac voltage from several levels of dc input voltages. Hence, multilevel inverters can easily provide the high power required in the aforementioned applications.

The result is the advent of the transformerless multilevel inverter topologies. Distinctly, three main types of transformerless multilevel inverters have been proposed in the literature, namely: the diode-clamp, the flying-capacitor, and the cascade multilevel inverters; [2] – [5]. In each of these configurations, there is the need to have a systematic outline of the switching states of the active device for a chosen number of phases and level of the inverter. In other words, a generalized truth table that gives all possible states of the multilevel inverter output with any number of phases need to be formulated.

The performance of the multilevel inverters depends largely on the control strategy employed. The most popular control strategy for multilevel inverter configurations is the Pulse Width Modulation (PWM) technique; which basically comprise of the carrier-based PWM [6]. Specific
Elimination PWM [4], and Space Vector PWM [7]. The Space Vector PWM is the most recent that received widespread attention, because it offers significant flexibility and high performance characteristics.

The performance/quality of any of these PWM techniques for a given multilevel inverter is measured by the harmonic profile of the inverter output voltage waveform/s. Though in the literature, recent works have used these PWM techniques on the multilevel inverter topologies [4], [6], [7], [8], [9], and [10]; but none gave a generalized format/pattern for the harmonic profile of the output voltage waveforms for a specified number of phase and level, as well.

In this work, description of the principles of operation of multilevel voltage source inverters is carried out. A generalized truth table for the switching states of multilevel inverters is formulated. The formulation gives all possible states of an inverter output phase during switching action. Fundamentally, the truth table shows distinctly the dc voltage level at which each active device in each phase of the inverter can be switched to for a desired output voltage waveform.

The Space vector modulated multilevel inverter has been treated in detail in this work. Using the switching state vector diagram for any given multilevel inverter, the optimum switching sequence for minimum switching loss is derived. Illustrations are given to show how the optimum sequence is determined for a given inverter output voltage level. The spectral profile of the inverter output voltage waveform under optimum switching operations is obtained by Fourier analysis for varying sampling periods. From the results, a generalized pattern of the harmonic profile of the inverter output voltage waveforms was derived. Also, the results show that as the sampling frequency ratio, R, increases, harmonics equal to or lower than the \((R-1)th\) harmonics order are eliminated.

The work is organized under six chapters. In chapter two, multilevel inverter topologies/configurations are presented. Switching states to give desired output voltage of any inverter phase are given. Generalized truth table of the multilevel of the multilevel inverter is formulated and illustrations given.

The PWM control schemes are described in chapter three. The Multi-carrier PWM is illustrated for 5-level inverter and the resultant inverter output voltage waveforms are presented. Switching vector diagrams for 2- to 5-level inverters are illustrated. The concept of space Vector modulation is presented and the transformation of the vector diagram representation into two coordinate axes are discussed. Using the transformation, the derivation
of the optimal switching sequences for the three–phase multilevel inverter are given.

In chapter four, the output voltage waveforms for unmodulated three–phase, 2–, 3–, 4–, and 5–level inverters are presented from their respective switching vector diagrams. Illustrative calculations are made to determine the optimal switching sequences for 3–phase, 3–level Space Vector modulated inverter, sampled at an angular distance of 60°. The resultant output voltage waveforms are drawn. Optimal switching sequences for various values of the sampling frequency are presented.

In chapter five, all the generated inverter output voltage waveforms are analyzed and the spectral profile presented.
CHAPTER TWO.

MULTILEVEL INVERTER TOPOLOGIES.

The magnetic transformer coupled multi-pulse voltage source inverter has been a well-known method. They typically synthesize the staircase voltage wave by varying the transformer turns ratio with complicated zigzag connections. Problems of these inverters are that they are bulky, heavy and loose. The capacitor voltage synthesis method is preferred to the magnetic coupling method [2]. Discussed under is the generalized multilevel inverter circuit configuration with self-voltage balancing.

2.1: GENERALIZED MULTILEVEL INVERTER TOPOLOGY WITH SELF-VOLTAGE BALANCING.

A generalized circuit layout, which allows the synthesis of the existing multilevel inverter topologies, is shown in fig.2.1, [3]. From fig. 2.1, it can be seen that each switching device, diode, or capacitor's voltage is \( V_{dc} \), i.e., \( 1/(M-1) \) of the dc-link voltage, where \( M \) indicates the level of the inverter. To explain the operating principle and analyze the circuit, the 5-level circuit is arbitrarily chosen. Fig.2.2 shows the generalized 5-level inverter phase leg. In this figure, switches \( S_{11} \) to \( S_{14} \), \( S_{31} \) to \( S_{34} \), \( D_{p1} \) to \( D_{p4} \), \( D_{n1} \) to \( D_{n4} \), shown in bold red lines are the main devices to produce the desired voltage waveforms. The rest of the switches and diodes are for clamping and balancing the capacitors' voltages, i.e., voltage levels. Each component's voltage stress is \( V_{dc} \). All voltage levels are self-balanced through clamping switches and diodes. The operation can be explained as in figs.2.3 to 2.5.

The circled (both solid and light lines) devices indicate on-state devices and current path. The uncircled ones are off-state devices. In addition, the solid-line circled devices are the on-state devices necessary to produce the desired voltage level; whereas the light line circled ones are the on-state devices to keep their capacitors' voltages balanced, i.e., for balancing and clamping purpose.
FIG. 2.1: GENERALIZED MULTILEVEL INVERTER TOPOLOGY (M-LEVEL, ONE PHASE LEG)
FIG. 2.2: FIVE-LEVEL INVERTER PHASE LEG.
FIG. 2.3: SWITCHING STATE TO PRODUCE $V_o = 0$ AND TO CLAMP/BALANCE CAPACITORS' VOLTAGES.
FIG. 2.4: SWITCHING STATE TO PRODUCE $V_0 = V_{dc}$ AND TO CLAMP/BALANCE CAPACITORS' VOLTAGES.
FIG. 2.5: Alternative switching state to produce $V_o = V_{dc}$ and to clamp/balance capacitors' voltages.
In Fig.2.3, switches $S_n$ to $S_{m}$ are gated on to produce zero voltage (i.e., $V_0 = 0$), the zero potential is referred to the negative rail of the dc bus. The light circled devices are gated on to clamp and balance voltages. The switches $S_{a}$, $S_{c}$, and $S_{d}$ are gated on so that the capacitors $C_1$, $C_3$, $C_6$, and $C_{10}$ are connected in parallel to balance their charges (i.e., $V_{c1} = V_{c3} = V_{c6} = V_{c10}$). Similarly, the switches $S_{a}$, $S_{b}$ are gated on so that $V_{c2} = V_{c5} = V_{c8}$. And $S_{c}$ is gated on letting $V_{o} = V_{dc}$.

Fig.2.4 shows one set of switching states for producing $V_0 = V_{dc}$. There are three other alternative switching states. In this figure, $V_{c1} = V_{c3} = V_{c6} = V_{c10}$; $V_{c2} = V_{c5} = V_{c8}$, and $V_{o} = V_{dc}$.

An alternative switching pattern to realize $V_0 = V_{dc}$ is shown in fig. 2.5. Here, $V_{c3} = V_{c6} = V_{c10}$; $V_{c2} = V_{c5} = V_{c8}$ and $V_{o} = V_{dc}$.

From the above explanation, one can infer the following switching rules:

1. Each switch pole is an independent switching unit.
2. Any adjacent two switches of each pole are complementary (i.e., if one is on, the other is off and vice versa).
3. If any switch state is determined, then the rest switches of the pole are automatically determined because of the complementary rule.

Table 2.1 summarizes the switching states to generate $0$, $1$, $2$, $3$, and $4$-$V_{dc}$ voltage levels.

**Table 2.1: Switching states to produce $V_0 = 0$, $1$, $2$, $3$, and $4$-$V_{dc}$ voltage levels.**

<table>
<thead>
<tr>
<th>Output voltage $V_{dc}$</th>
<th>Capacitor path*</th>
<th>Switch States**</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 $V_{dc}$</td>
<td>None</td>
<td>$S_{a}$ $S_{b}$ $S_{c}$ $S_{d}$ $S_{a}$ $S_{b}$ $S_{c}$ $S_{d}$</td>
</tr>
<tr>
<td></td>
<td>$+C1$</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td></td>
<td>$-C1 + C2 + C3$</td>
<td>0 0 0 0 1 1 1 1</td>
</tr>
<tr>
<td></td>
<td>$-C3 + C2 + C4 + C5 + C6$</td>
<td>0 0 1 0 0 0 0 0</td>
</tr>
<tr>
<td></td>
<td>$-C6 + C5 + C4 + C7 + C8 + C9 + C10$</td>
<td>0 0 0 0 1 1 1 1</td>
</tr>
<tr>
<td>$2V_{dc}$</td>
<td>$+C2 + C3$</td>
<td>1 1 1 0 0 0 0 1</td>
</tr>
<tr>
<td></td>
<td>$-C1 + C4 + C5 + C6$</td>
<td>1 1 1 0 0 0 0 1</td>
</tr>
<tr>
<td></td>
<td>$-C1 + C2 + C7 + C8 + C9 + C10$</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td></td>
<td>$+C1 + C3 + C2 + C4 + C5 + C6$</td>
<td>1 0 1 0 0 0 0 1</td>
</tr>
<tr>
<td></td>
<td>$+C1 + C6 + C5 + C4 + C7 + C8 + C9 + C10$</td>
<td>1 0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>
The capacitor path shows those capacitors that are connected to the output for each correspondent switching states. "+" shows that the capacitor is connected positively to the output and "-" shows that the capacitor is connected negatively.

**"1" indicates an and "0" indicates off-state.**

### 2.2: DIODE-CLAMPED MULTILEVEL INVERTERS.

An M-level diode-clamped converter typically consists of M-1 capacitors on the dc bus and produces M-level of the phase voltage. For an illustration, a 5-level diode-clamped inverter is realized from Fig. 2.2 by eliminating clamping switches and capacitors. The dc bus consists of four capacitors C1, C2, C3, and C4. For a dc bus voltage of $V_{dc}$, the voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes; consider Fig. 2.6.

To explain how the staircase voltage is synthesized, the negative dc rail, 0, is considered as the output phase voltage reference point. From this figure, there are five switch combinations to synthesize five level voltages across 1 and 0.

1. For voltage level $V_{ao} = V_{dc}$, turn on all upper switches $S_{a1}$ through $S_{a4}$.
2. For voltage level $V_{ao} = 3V_{dc}/4$, turn on three switches through $S_{a3}$ and one lower switch $S_{a4}$.
3. For voltage level $V_{ao} = V_{dc}/2$, turn on two upper switches $S_{a1}$ and $S_{a2}$ and two lower switches $S_{a3}$ and $S_{a4}$.
4. For voltage level $V_{ao} = V_{dc}/4$, turn on one upper switches $S_{a1}$ and...
three lower switches $S_{a1}$ through $S_{a3}$

5. For voltage level $V_{ao} = 0$, turn on all lower switches $S_{a1}$ through $S_{a3}$.

Table 2.2 lists the voltage levels and their corresponding switch states.

**Table 2.2: Switching states to produce $V_{ao} = V_{dc}/4, V_{dc}/2, V_{dc}/4$ and $0$ Voltage levels.**

<table>
<thead>
<tr>
<th>Output Voltage $V_{ao}$</th>
<th>$S_{a1}$</th>
<th>$S_{a2}$</th>
<th>$S_{a3}$</th>
<th>$S_{a4}$</th>
<th>$S_{a4'}$</th>
<th>$S_{a5}$</th>
<th>$S_{a5'}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ao} = V_{dc}$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_{ao} = 3V_{dc}/4$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_{ao} = V_{dc}/2$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$V_{ao} = V_{dc}/4$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$V_{ao} = 0$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

It can be noticed that each switch is only switched once per cycle. There exist four complementary switch pairs. The complementary switch pair is defined such that turning on one of the pair switch will exclude the other from being turned on. The four complementary pairs are $(S_{a2}, S_{a4'})$, $(S_{a2}, S_{a2'})$, $(S_{a3}, S_{a5})$, and $(S_{a4}, S_{a5'})$.

Another circuit configuration for single-phase, 5-level diode-clamped multilevel converter is shown in fig. 2.7.
FIG. 2.6: DIODE-CLAMPED, PHASE-LEG, 5-LEVEL INVERTER.
FIG. 2.7: SINGLE-PHASE, 5-LEVEL DIODE-CLAMP INVERTER.
Features of this configuration are:

1. **High voltage rating required for blocking diodes:** Although each active device is only required to block a voltage level of $V_{dc}/(M-1)$, the clamping diodes need to have different voltage rating for reverse voltage blocking. Using $D_{cl}$ in fig.2.6 as an example, when all lower switching devices are on, $D_{cl}$ need to block three capacitor voltages, or $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required will be $(M-1)^2 (M-2)$. This number represents a quadratic increase in M. When M is sufficiently high, the number of diodes required will make the system impractical to implement.

2. **Unequal device rating:** From table 2.2, it can be seen that $S_{in}$ conducts only when $V_{in} = V_{dc}$, while switch $S_{out}$ conducts over the entire cycle except during $V_{in} = 0$. Such an unequal conduction duty requires different current rating for the switching devices. When the inverter design is to use the average duty of all devices, the outer switches may be oversized and the inner switches undersized. If the design is to suit the worst case, then there will be $2(M-2)$ outer devices oversized.

### 2.3: MULTILEVEL INVERTERS USING FLYING CAPACITORS

Elimination of the clamping switches and diodes from the generalized circuit topology of fig.2.2 result in another circuit configuration – the capacitor-clamped (or flying capacitor) multilevel inverter shown in fig.2.8. The voltage level defined in the flying capacitor multilevel converter is similar to that of the diode-clamped type, but with more flexibility in switching pattern.

For the 5-level case as illustrated in fig.2.8, output $V_o$ can be synthesized by the following switch combination:

1. For voltage level $V_o = V_{dc}$, turn on all upper switches $S_{out}$ through $S_{st}$.
2. For voltage level $V_o = 3V_{dc}/4$, there are four combinations.
   a. $S_{out}, S_{st}, S_{in}, S_{out}$ ($V_o = V_{dc} - V_{st}/4$)
   b. $S_{st}, S_{in}, S_{st}, S_{out}$ ($V_o = 3V_{dc}/4$)
   c. $S_{out}, S_{st}, S_{out}, S_{out}$ ($V_o = V_{dc} - 3V_{dc}/4 + V_{st}/2$) and
   d. $S_{st}, S_{out}, S_{out}, S_{st}$ ($V_o = V_{dc} - V_{st}/2 + V_{st}/4$)
3. For voltage level $V_o = V_{dc}/2$, there are six combinations.
   a. $S_{out}, S_{st}, S_{st}, S_{out}$ ($V_o = V_{dc} - V_{st}/2$)
4. For voltage level $V_a = V_{dc}/4$, there are four combinations.
   a. $S_{a1}$, $S_{a2}'$, $S_{a4}'$ ($V_a = V_{dc}/3V_{dc}/4$)
   b. $S_{a1}$, $S_{a2}'$, $S_{a3}'$, $S_{a4}'$ ($V_a = V_{dc}/4$)
   c. $S_{a1}$, $S_{a4}'$, $S_{a2}'$, $S_{a3}'$ ($V_a = V_{dc}/2 - V_{dc}/4$) and
   d. $S_{a2}$, $S_{a3}'$, $S_{a4}'$, $S_{a1}'$ ($V_a = 3V_{dc}/4 - V_{dc}/4$)

5. For voltage level $V_a = 0$, turn on all lower switches $S_{a1}'$ through $S_{a4}'$.

Table 2.3: Switching states to produce $V_a = V_{dc}/4$, $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$ and $0$ Voltage levels

<table>
<thead>
<tr>
<th>Output Voltage $V_a$</th>
<th>$S_{a1}$</th>
<th>$S_{a2}$</th>
<th>$S_{a3}$</th>
<th>$S_{a4}$</th>
<th>$S_{a1}'$</th>
<th>$S_{a2}'$</th>
<th>$S_{a3}'$</th>
<th>$S_{a4}'$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V = V_{dc}$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V = 3V_{dc}/4$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V = V_{dc}/2$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V = V_{dc}/4$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$V = 0$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
FIG. 2.8: CAPACITOR-CLAMPED, (OR FLYING CAPACITOR) PHASE-LEG, 5-LEVEL INVERTER.
FIG. 2.9: SINGLE-PHASE, 5-LEVEL FLYING-CAPACITOR INVERTER.
Using such switch combinations, each device needs to be switched only once per cycle. According to the device turn-on time requirement listed in table 2.3, the flying-capacitor multilevel inverter also has unequal device duty problem. Besides, another problem in this inverter configuration is the requirement of a large number of storage capacitors. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an M-level inverter will require a total of \((M-1)^2(M-2)/2\) auxiliary capacitors. With the assumption that all capacitors have the same voltage rating, an M-level diode-clamped converter only requires \((M-1)\) capacitors [11]. Fig.2.9 shows another circuit arrangement for single-phase, 5-level flying-capacitor multilevel inverter.

2.4 MULTILEVEL INVERTERS EMPLOYING CASTACDED INVERTERS WITH SEPARATE DC SOURCES, SDCS.

The cascaded H-bridge inverters or simply the cascaded inverters inherently does not make use of clamping diodes or capacitors, rather it consists of a series of single-phase, full-bridge inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCS), which may be obtained from batteries, fuel cells or solar cells. Fig.2.10 shows a generalized single-phase structure of a cascaded inverter with SDCS.

Each SDCS is connected to a single-phase, full-bridge inverter. Each inverter level can generate three different voltage outputs \((0, +V_{dc}, -V_{dc})\) by connecting the dc source to the ac side by different combinations of the four switches, \(S_1, S_2, S_3,\) and \(S_4\). The ac outputs of each of the different level full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

\[
M = 2S + 1
\]

Where \(S\) is the number of dc sources [4].
FIG. 2.10: GENERALIZED SINGLE-PHASE STRUCTURE OF CASCADED H-BRIDGE INVERTER WITH SDCS.
FIG. 2.11: SINGLE-PHASE STRUCTURE OF 9-LEVEL CASCADED H-BRIDGE INVERTER WITH SDCS.
FIG. 2.11: SWITCHING PATTERN OF THE 9-LEVEL CASCADED INVERTER.
FIG. 2.12: PHASE VOLTAGE WAVEFORM OF 9-LEVEL CASCaded INVERTER.
For an illustration, from fig. 2.10 and with reference to equation (2.1), the circuit layout for single-phase, 9-level cascaded inverter is shown in fig. 2.11. The circuit comprise of four single phase, full-bridge inverters with separate dc sources connected in series. Fig. 2.12 shows any of these full-bridge inverters, the gating signals of the active switches and the resultant voltage output. The switching sequence is summarized in the table below.

<table>
<thead>
<tr>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>Output voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>$-V_{dc}$</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>0</td>
</tr>
<tr>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>0</td>
</tr>
</tbody>
</table>

Hence, a quasi-square waveform is obtained at the output of each of the single phase, full-bridge inverter. The pulsewidths of these waveforms are determined by the delay angle, $\theta_i$, of the switch $S_i$ in each of these inverters. The phase voltage of the 9-level cascaded inverter is the sum of the individual output voltage of the four single phase, full-bridge inverters; $V_{m} = V_{s1} + V_{s2} + V_{s3} + V_{s4}$.

In effect, the delay angle $\theta_1 - \theta_4$ in each of the full-bridge inverters are carefully chosen so that the algebraic sum of the output voltages of these inverters results in a staircase output voltage waveform for the cascaded inverter shown in fig. 2.13. It should be noted that in fig. 2.13, each switching device always conducts for 180° (or $\frac{1}{4}$ cycle), regardless of the pulse width of the quasi-square wave. This switching method makes all of the active devices' current stress equal. The features of this multilevel inverter configuration are:

1. it is most suitable for high voltage, high power application than the aforementioned multilevel inverters; as the structure of the SDCS is well suited for various renewable energy sources, such as fuel cell, photovoltaic, and biomass, etc.

2. The topology requires the least number of components amongst all multilevel inverters to achieve the same number of voltage levels.

3. Since the inverter structure itself consists of cascade connection of many single-phase inverter units, and each bridge is fed with a SDCS, it does not require voltage balancing (sharing) circuits or voltage matching of the switching devices.

4. Modularized circuit layout and packaging is possible because each level has the same structure.
5. Soft switching can be used in this topology to avoid bulky and loose resistor-capacitor-diode snubbers [12].

2.5 GENERALIZED TRUTH-TABLE REPRESENTATION OF MULTILEVEL INVERTER SWITCHING STATES.

All the switching states of an M-level inverter can be realized and tabulated (i.e., truth-table), from the basic facts that for an M-level, \( \phi \)-phase inverter, the possible number of switching states is given by

\[
N = M^\phi
\]

And the switching state range is

\[
R = 0 \text{ to } (M-1)
\]

For a specified number of inverter level and phase, the corresponding number of columns of the truthtable equals the number of phases of the multilevel inverter system. The number of rows of the truthtable equals the number of possible switching states, given by equation (2.2). Hence, the truthtable is formulated starting from the last towards the first column. The range (0 to M-1) is repeated up to \( M^\phi \) times in the last column; the subsequent columns start with the zero (0) switching state and change to 1, 2, \ldots, \( M-1 \) switching states only when the range (0 to M-1) is repeated in the immediate preceding column.

To illustrate the truth-table representation, the 3-level, 3-phase; 3-level, 4-phase; and 4-level, 3-phase multilevel inverters were chosen arbitrarily. Their truth-tables are presented below.

\[3\text{-level, 3-phase inverter:}\]

The number of switching state is \( N = M^\phi \) i.e., \( 3^3 = 27 \) states; and the range, \( R = 0 \text{ to } (M-1) \Rightarrow 0 \text{ to } (3-1) \Rightarrow 0 \text{ to } 2 \), i.e., 0, 1, 2. Hence the truth-table is

<table>
<thead>
<tr>
<th>Table 2.4: 3-level, 3-phase inverter truth-table.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>
ii. 3-level, 4-phase inverter: The number of switching state is $N = M^3$ i.e., $3^3 = 27$ states; and the range, $R = 0$ to $(M-1) \Rightarrow 0$ to $(3-1) \Rightarrow 0$ to 2, i.e., 0, 1, 2. Thus, the truth-table is

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>0</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2.5: 3-level, 4-phase inverter truth-table.
iii. 4-level, 3-phase inverter: The number of switching state is $N = M^3$ i.e., $4^3 = 64$ states; and the range, $R = 0$ to $(M-1) \Rightarrow 0$ to $(4-1) \Rightarrow 0$ to 3, i.e., 0, 1, 2, 3. Thus, the truth-table is

Table 2.6: 4-level, 3-phase inverter truth-table.

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>11</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>12</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>13</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>14</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>15</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>
Amongst the various control schemes for the so far discussed inverter configurations, multi-carrier, Specific Harmonic Elimination, and space vector pulse width modulation, pwm, techniques are predominantly used. In the discussions that follow, the basic principles and operations of each of these pwm control strategies are presented.

### 3.1 SUB-HARMONIC/MULTI-CARRIER PWM STRATEGY.

Multi-carrier pwm techniques entail the natural sampling of a single modulating or reference waveform, typically being sinusoidal, through several multilevel carrier signals, typically being triangular waveform. Multilevel sub-harmonic pwm (SHPWM) can be developed as follows, [6]. For an M-level inverter, M-1 carriers with the same frequency, $f$, same peak-to-peak amplitude, $A_n$, are disposed such that the bands they occupy are contiguous. The reference, or modulating waveform has peak-to-peak amplitude, $A_m$, and frequency, $f_m$, and is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signal. If the reference is greater than the carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than the carrier signal, the corresponding active device is switched off.

Multi-carrier pwm is classified into two [7]: carrier disposition and phase-shift (PS), multi-carrier pwm methods. The disposition is further classified as: Alternate Phase Opposition disposition (APOD), Phase disposition (PD), and Phase opposition disposition (POD) modulations.

The frequency modulation index is defined as $m_f = f / f_m$, while the amplitude modulation index, $m_a$, is defined for each modulation technique in Table 3.1 below.

<table>
<thead>
<tr>
<th>$m_a$</th>
<th>APOD</th>
<th>POD</th>
<th>PD</th>
<th>PS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_m / ((M-1)/2)^*$</td>
<td>$A_m / ((M-1)/2)^*$</td>
<td>$A_m / ((M-1)/2)^*$</td>
<td>$A_m / A_c$</td>
<td></td>
</tr>
</tbody>
</table>

For each technique, the following parameters introduce degree of freedom:
The frequency modulation index, $n_f$.

b. The amplitude modulation index, $m_a$.

c. The angle, $\phi$, of displacement between the modulating signal (sinusoidal) and the first positive triangular signal. In this work, only $\phi = 0$ is applied.

3.11 CARRIER DISPOSITION METHODS.

In this category of multi-carrier PWM techniques, the reference is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform amplitude. Included in this category are the APOD, PD, and POD pulse width modulations.

3.111 Alternate Phase Opposition disposition (APOD) modulation.

For an M-level inverter, this technique requires each of the M-1 carrier waveforms to be phase displaced from each other by 180° alternately. To illustrate this modulation strategy, Fig. 3.1 shows the modulating and carrier waveforms for 5-level converter for amplitude modulation index, $m_a = 0.8$, and frequency modulation index, $n_f = 20$.

The inverter 5-level phase voltage is also shown.

3.112 Phase disposition (PD) modulation.

This technique is similar to the previously described modulation above, i.e., APOD, except that all carriers are in phase. Fig. 3.2 illustrates this modulation strategy.

3.113 Phase Opposition disposition (POD) modulation.

Here, the carrier waveforms are all in phase above and below the zero reference value; however, there is 180° phase shift between the ones above and below zero reference point. Fig. 3.3 typifies this very modulation technique.

It should be remarked that the above discussed multi-carrier disposition modulation are best suited for the control of multilevel diode-clamped converter configuration [7].

3.12 PHASE-SHIFT MULTI-CARRIER (PS) PWM METHOD.

This modulation technique employs a number of carriers, which are all phase-shifted accordingly. The carrier phase shift is given by [8]

$$180°/(\text{number of dc sources per phase})$$

(3.1)
To illustrate this modulation process, consider a 5-level converter system; hence from equation (2.1)

\[ M = 2^{(S+1)} \]

\[ \Rightarrow S = \frac{(M-1)}{2} \Rightarrow \frac{(5-1)}{2} = 2. \]

Therefore, for this level of inverter employing this modulation technique, the \((M-1)\), i.e., 4 carriers are phase shifted from one another by \(180^\circ/2 = 90^\circ\), accordingly. Fig. 3.4 fully illustrate this very modulation technique.

It should be noted that while the level used for the so far discussed multi-carrier PWM is five, for illustrative purposes; the same pattern of modulation process is applicable for high levels.
FIG. 3.1: ALTERNATE PHASE OPPOSITION (APOD) MULTI-CARRIER PWM; $M_f = 20, M_a = 0.8, m = 5.$
PHASE DISPOSITION
MULTICARRIER PWM;
$M_f = 20, M_a = 0.8, m = 5$.

---

FIG. 3.2: PHASE DISPOSITION (PD) MULTI-CARRIER PWM; $M_f = 20, M_a = 0.8, m = 5$.
PHASE OPPOSITION DISPOSITION (POD) MULTICARRIER PWM; $M_f = 20$, $M_a = 0.8$, $m = 5$.

FIG. 3.3: PHASE OPPOSITION DISPOSITION (POD) MULTICARRIER PWM; $M_f = 20$, $M_a = 0.8$, $m = 5$. 

$M_f$: Fundamental frequency
$M_a$: Modulation index
$m$: Number of carriers
FIG. 3.4: PHASE SHIFT (PS) MULTI-CARRIER PWM; $M_f = 20$, $M_a = 0.8$, $m = 5$. 

PHASE SHIFT (PS) MULTICARRIER PWM; $M_f = 20$, $M_a = 0.8$, $m = 5$. 

FIG. 3.4: PHASE SHIFT (PS) MULTI-CARRIER PWM; $M_f = 20$, $M_a = 0.8$, $m = 5$. 

37
3.2: SPECIFIC HARMONIC ELIMINATION PWM TECHNIQUE.

With reference to fig. 2.13, such stepped-waveform with S steps has the Fourier transform as follows, [4]:

\[ V(n) = 4V_{dc}/\pi \sum_{n=1}^{\infty} \left[ \cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s) \right] \sin(n\omega t)/n \]

Where \( n = 1, 3, 5, 7, \ldots \) ------- (3.2).

The magnitudes of the Fourier coefficients when normalized with respect to \( V_{dc} \) are as follows:

\[ H(n) = 4/n \pi \left[ \cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s) \right] \]

Where \( n = 1, 3, 5, 7, \ldots \) ------- (3.3).

The conducting angles \( \theta_1, \theta_2, \ldots, \theta_s \) can be chosen such that the average total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [3], [9].

It is necessary to state that the Specific Harmonic Elimination and phase-shift multi-carrier (PS) PWM techniques are best adapted for multilevel inverters using cascaded inverters with separate dc sources [4], [8].

3.3: SPACE VECTOR PWM FOR M-LEVEL CONVERTER.

Ever since the introduction of the concept of multilevel pulse width modulation, PWM, inverter [13], various modulation techniques, some of which have been discussed in the preceding subchapters above, have been developed. Among these control strategies, space vector modulation (SVM) stands out; basically because it offers significant flexibility to optimize switching waveforms [10]; and because it is well suited for implementation on a digital computer.

Space vector modulation identifies each switching state of a multilevel inverter as a point in complex space. Then, a reference phasor rotating in the complex plane at the fundamental frequency is sampled within each switching period; and the nearest three inverter switched states are selected with duty cycles calculated to achieve the same volt-second average as the sampled reference phasor. This directly controls the inverter line-to-line voltages, and only implicitly develops the phase leg voltages. Very recent works have shown how to do these calculations for a generalized M-level diode-clamped inverter and also gave insight into the optimal sequence of space vector states and the method’s applicability to other multilevel inverter topologies [14], [15].
Thus, the rudimentary steps involved in the SVM process are presented as follows.

3.3.1: VECTOR REPRESENTATION.
For a three-phase multilevel inverter, each phase can be modeled as an M-pole switch as shown below.

Fig. 3.5: functional diagram of M-level, Three-phase inverter.

Fig. 3.5 shows the functional diagram of an M-level, three-phase inverter in which the single-pole M-throw switches represent the functionality of each inverter phase. Regardless of the number of inverter level, every switching state produces uniquely defined three-phase line voltages, which can be represented as vectors in three-dimensional Euclidean vector space. For an instance, if the location of the equivalent phase switches of the phases a, b, c were in the positions i, j, k, respectively, where $i, j, k \in [0, 1, 2, \ldots, M-1]$, then that switching state could be represented with the switching vector

$$V_{(i,j,k)} = V_{dc} [i-j \ j-k \ k-i]^T \hspace{1cm} (3.4)$$
At this juncture, it is necessary to put down some hints that will help in the understanding of the space vector representation.

For an M-level inverter, the number of switching states, N, from equation (2.2) is given by

\[ N = M^4 \]

where \( M \) and \( \phi \) are the number of level and phase, respectively. In these numbers of switching states, there exist active and redundant switching states. Active switching states are those inverter-switching states that give unique and distinct space vectors; while the redundant states are inverter-switching states that give the same space vector.

Now, the number of redundant space vectors for an M-level inverter is generally given by

\[ N_R = (M-1)^4 - (M-2)^4 \]

(3.5)

It then follows that the number of active switching vectors is also given by

\[ N_A = N - N_R \]

From equation (3.4), each space vector, representing the line voltages, is formed from the possible combinations of the \( i, j, k \) assumed values in each modeled M-throw pole switch in the phases.

Taking a particular case of a three-phase system (i.e., \( \phi = 3 \)), equations (2.2), (3.4), (3.5), and (3.6) become

\[ N = M^3 \]

(3.7)

\[ N_R = (M-1)^3 - (M-2)^3 \]

\[ \Rightarrow 3M^2 - 9M + 7 \]

(3.8)

\[ N_A = \{M^3 - [(M-1)^3 - (M-2)^3]\} \]

\[ \Rightarrow M^3 - 3M^2 + 9M - 7 \]

(3.9)

Shown in figs.3.6, 3.7, 3.8, and 3.9 are all the switching vectors of a three-phase, 2-, 3-, 4-, and 5-level multilevel inverters, respectively; with their positions of the equivalent phase switches (i.e., the switching states).

It can be noticed that the structure of the hexagon changes when the number of inverter level is increased from two, three, four to five. Increasing the number of level by one always forms an additional hexagonal ring of equilateral triangles, which surround the outermost hexagon.

Similarly, a reference vector in steady state can also be represented in vector form as
FIG. 3.7: SWITCHING VECTORS OF THREE-PHASE, THREE-LEVEL INVERTER.
FIG. 3.6: SWITCHING VECTORS OF THREE-PHASE, TWO-LEVEL INVERTER.
FIG. 3.8: SWITCHING VECTORS OF THREE-PHASE, FOUR-LEVEL INVERTER.
FIG. 3.9: SWITCHING VECTORS OF THREE-PHASE, FIVE-LEVEL INVERTER.
Using the definition of vector norm, the length of the reference vector is

\[ |\vec{V}_{\text{ref}}| = \sqrt{(\vec{V}_{\text{ref}} \cdot \vec{V}_{\text{ref}})} \]

\[ = \sqrt{V_{L-L}^2} \]

Also using the same definition, the length of the largest voltage space vector is

\[ |\vec{V}_{\text{max}}| = \sqrt{[2(M-1)] V_{dc}} \]

The maximum length of the reference vector that can be synthesized equals the radius of the largest circle that can be inscribed in the outermost hexagon. Therefore, the maximum length of the reference vector for a general multilevel inverter is

\[ |\vec{V}_{\text{ref, max}}| = |\vec{V}_{\text{max}}| * \cos(\pi/6) \]

By substituting equations (3.11) and (3.12) into (3.13), the maximum amplitude of the undistorted line-to-line voltage that a multilevel inverter can synthesize is

\[ V_{L-L, \text{max}} = (M-1) V_{dc} \]

3.32: COORDINATE TRANSFORMATION.

In order to determine which position the switches should assume (switching states), and the duration needed (duty cycle) so that the reference voltage vector can be synthesized, the concept of the 'Three Nearest Vector' is used:

\[ \vec{V}_{\text{ref}} = d_1 \vec{V}_1 + d_2 \vec{V}_2 + d_3 \vec{V}_3 \]

Because of the computational difficulty involved as the number of levels increases, the selection of three nearest vectors and the computation of their
duty cycles are better performed if the reference voltage vector and also the voltage space vectors are transformed into two-dimensional coordinate system using a coordinate transformation matrix

\[ V_{ref}(ab) = T \cdot V_{ref} (V_a, V_b, V_{ab}) \]  

(3.16)

One such transformation matrix that also normalizes the length of vectors with the lengths of the basis vector is

\[
\begin{pmatrix}
2 & -1 & -1 \\
-1 & 2 & -1
\end{pmatrix}
\]  

(3.17)

Shown in fig.3.10 is a two-dimensional representation of the reference vector and the voltage space vectors from fig.3.7.


Having successfully transformed into the two-dimensional plane, the next task is detection of the nearest three vectors that approximate the reference vector.

To clearly understand the detection process, it is better to consider a typical case. Considering fig.3.10, it can be seen that the reference voltage vector falls inside an equal-sided parallelogram, whose coordinates are marked with asterisks (*). Upper and lower sides of this parallelogram are designated U and L respectively. Hence, \( V_{UL}, V_{LU}, V_{UU}, V_{LL}, \) are defined as follows:

- \( V_{UL} \) = Voltage vector whose coordinates are at the right, lower side of the parallelogram.
- \( V_{LU} \) = Voltage vector whose coordinates are at the left, upper side of the parallelogram.
- \( V_{UU} \) = Voltage vector whose coordinates are at the right, upper side of the parallelogram.
- \( V_{LL} \) = Voltage vector whose coordinates are at the left, lower side of the parallelogram.
FIG. 3.10: SWITCHING-STATE VECTORS OF THREE-LEVEL INVERTER IN HEXAGONAL COORDINATE SYSTEM.
With this definitions therefore, the parallelogram under consideration has end voltage vectors:
\[
V_{dl} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad V_{dl'} = \begin{bmatrix} -1 \\ 2 \end{bmatrix}, \quad V_{dl''} = \begin{bmatrix} 0 \\ 2 \end{bmatrix}, \quad V_{dl'''} = \begin{bmatrix} 1 \\ 1 \end{bmatrix}.
\]

It should be noted that as the reference voltage vector rotates during each sampling period, it falls into similar parallelogram and \( V_{dl'}, V_{dl''}, V_{dl'''} \), can easily be identified.

Hence, the end points of the nearest four vectors form the equal-sided parallelogram that is divided into two equal-sided triangles by the diagonal connecting vectors \( V_{dl'} \) and \( V_{dl''} \). The vectors \( V_{dl'} \) and \( V_{dl''} \) are always two of the nearest three vectors. The third nearest vector can be found by evaluating the sign of the expression:
\[
V_{ref, g} + V_{ref, h} \cdot (V_{dl', g} + V_{dl'', h}),
\]
where
\[
V_{ref, g} = \text{g component of } V_{ref},
V_{ref, h} = \text{h component of } V_{ref},
V_{dl', g} = \text{g component of } V_{dl'},
V_{dl', h} = \text{h component of } V_{dl'}.
\]
If the sign is positive, the vector \( V_{dl'''} \) is the third nearest vector; otherwise, vector \( V_{dl''} \) is the third nearest vector. This completes the identification of the nearest three vectors for the M-level inverter.

### 3.34: DUTY CYCLE COMPUTATION.

Once the nearest three vectors are identified, their corresponding duty cycles can be found by solving equation (3.15), where
\[
V_{1} = V_{dl'}, \quad V_{2} = V_{dl''}, \quad V_{3} = V_{dl'''} \quad V_{4} = V_{dl''}, \quad \text{with the additional constraint}
\]
\[
d_1 + d_2 + d_3 = 1 \quad \text{---------} \quad \text{(3.19)}
\]

Fortunately however, because all switching state vectors always have integer coordinates, the solutions are essentially the fractional parts of the
\[
V_{ref} \text{ coordinates}
\]
\[
d_{11} = V_{ref, g} - V_{dl', g},
\]
\[
d_{12} = V_{ref, h} - V_{dl', h},
\]
\[
d_{11} = 1 - d_{11}, \quad d_{11} \quad \text{---------} \quad \text{(3.20)}
\]

48
3.35: SWITCHING STATE SELECTION.

This step requires a transformation from two-dimensional coordinate space back to the three-dimensional space of switching combinations. Choosing the best switch state or states at any given moment demands finding all the available switching states that can be represented with the same switching vector \( V_3 = [g, h] \). One way of finding these states is by evaluating

\[
\begin{align*}
\text{If } V_3 &= V_{1L}, \quad V_j = V_{1L}^r \\
\text{OR} \\
d_{1L} &= (V_{ref} - V_{1L}) \\
d_{IL} &= (V_{ref} - V_{1U}) \\
d_{L1} &= 1 - d_{1L} - d_{IL} \\
\text{If } V_3 &= V_{1U}, 
\end{align*}
\]

3.36: OPTIMIZED SPACE VECTOR SEQUENCES.

The final task is how to sequence or place the three nearest vectors in the switching period so as to minimize the total number of switching transitions. For a three-phase inverter, the minimum number of switching transitions in one switching cycle under continuous modulation is three (i.e., one per phase leg), so that the inverter cycles through four switched states in each switching period. At least the first and last of these must be redundant space vector states if only the three nearest space vectors are to be used.

Depending on where the reference phasor is located, there are two alternatives for this sequence:

1. Select two vectors of even redundancy and one vector of odd redundancy, or

\[
\begin{align*}
k & \quad k - g \\
k - g - h \\
\end{align*}
\]

Where \( k, k-g, k-g-h \in [0, 1, 2, M-1] \).
ii. Select one vectors of even redundancy and two vectors of odd redundancy.

With this very fact, optimal sequence of space vectors is better captured through practical illustration.

A subset of a 5-level space vector plot, and a table that summarizes all possible sequences for this subset are shown below.
Table 3.2: Possible switching state sequences for a subset of 5-level space vector plot.

<table>
<thead>
<tr>
<th>Triangle</th>
<th>Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>i. [432 to 431 to 421 to 321]</td>
</tr>
<tr>
<td></td>
<td>ii. [210 to 310 to 320 to 321]</td>
</tr>
<tr>
<td></td>
<td>iii. [421 to 321 to 320 to 310]</td>
</tr>
<tr>
<td></td>
<td>iv. [431 to 421 to 321 to 320]</td>
</tr>
<tr>
<td>(b)</td>
<td>i. [421 to 420 to 320 to 310]</td>
</tr>
<tr>
<td>(c)</td>
<td>i. [421 to 420 to 320 to 310]</td>
</tr>
<tr>
<td></td>
<td>ii. [431 to 421 to 420 to 320]</td>
</tr>
<tr>
<td>(d)</td>
<td>i. [431 to 430 to 420 to 320]</td>
</tr>
</tbody>
</table>

For triangles (b) and (d), there is only one possible sequence. For triangles (a) and (c), the correct sequence can be identified from the possible alternatives by ensuring that no extra switching transition occurs when moving between triangles. Hence, sequence c(i) should be used when moving from triangle (b) to (c), since it begins with the same state as in (b); or sequence c(ii) should be used when moving from triangle (c) to (d). Moreover, applying the same principle to triangle (a) means that sequence a(i) and a(ii) cannot be used because they will introduce extra switching transition when moving into triangle (c). Sequence a(iii) should be used when moving from triangle (a) to (b).

From the above explicitly discussed steps (coordinate transformation to optimized space vector sequencing), one will be in position of carrying out a space vector multilevel PWM for at least 3-level for a specified reference voltage vector and sampling period. Chapter four that follows explores this possibility.
CHAPTER FOUR.

SAMPLE CALCULATIONS.

In a bid to verify the performance of the space vector pulse width modulation technique, it becomes necessary to generate unmodulated voltage waveforms and also modulated signals with this modulation strategy.

4.1: UNMODULATED 3-PHASE, 2-LEVEL INVERTER.

With reference to fig. 3.6, the coordinates of the edges of the hexagonal ring form the switching state vectors of unmodulated 3-phase, 2-level inverter.

Normalization of equation (3.4) with the dc bus voltage ($V_{dc}$), result in

$$V_{k,i} = \begin{bmatrix} i-j & j-k & k-i \end{bmatrix}$$

(4.1)

Also, each voltage step has a conduction angle of $(360/6)° = 60°$. Hence, the line-to-line voltage ($V_{ab}$) steps with their corresponding conduction angles are tabulated under.

Table 4.1: line-to-line voltage ($V_{ab}$) steps of unmodulated 3-phase, 2-level inverter with their corresponding conduction angles.

<table>
<thead>
<tr>
<th>Voltage step (p.u)</th>
<th>Conduction angle (degrees)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>0 to 60</td>
</tr>
<tr>
<td>-1</td>
<td>60 to 120</td>
</tr>
<tr>
<td>0</td>
<td>120 to 180</td>
</tr>
<tr>
<td>1</td>
<td>180 to 240</td>
</tr>
<tr>
<td>1</td>
<td>240 to 300</td>
</tr>
<tr>
<td>0</td>
<td>300 to 360</td>
</tr>
</tbody>
</table>

4.2: UNMODULATED 3-PHASE, 3-LEVEL INVERTER.

Referring to fig. 3.7, the coordinates of the outer hexagonal ring form the switching state vectors of unmodulated 3-phase, 3-level inverter.
Application of equation (4.1) and bearing in mind that each voltage step has a conduction angle of \((360/12)^\circ = 30^\circ\), the line-to-line voltage \((V_{ab})\) steps with their corresponding conduction angles are tabulated below.

<table>
<thead>
<tr>
<th>Voltage step (p.u)</th>
<th>Conduction angle (degrees)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2</td>
<td>0 to 30</td>
</tr>
<tr>
<td>-1</td>
<td>30 to 60</td>
</tr>
<tr>
<td>-1</td>
<td>60 to 90</td>
</tr>
<tr>
<td>0</td>
<td>90 to 120</td>
</tr>
<tr>
<td>1</td>
<td>120 to 150</td>
</tr>
<tr>
<td>2</td>
<td>150 to 180</td>
</tr>
<tr>
<td>2</td>
<td>180 to 210</td>
</tr>
<tr>
<td>2</td>
<td>210 to 240</td>
</tr>
<tr>
<td>1</td>
<td>240 to 270</td>
</tr>
<tr>
<td>0</td>
<td>270 to 300</td>
</tr>
<tr>
<td>0</td>
<td>300 to 330</td>
</tr>
<tr>
<td>-1</td>
<td>330 to 360</td>
</tr>
</tbody>
</table>

**Table 4.2: line-to-line voltage (V_{ab}) steps of unmodulated 3-phase, 3-level inverter with their corresponding conduction angles.**

4.3: UNMODULATED 3-PHASE, 4-LEVEL INVERTER.

Fig. 3.8 shows the space vector diagram of the switching state vectors of 3-phase, 4-level inverter. The coordinates of the outer hexagonal ring of this diagram form the switching state vectors of unmodulated 3-phase, 4-level inverter. Each of the line-to-line voltage \((V_{ab})\) step has conduction angle of \((360/18)^\circ = 20^\circ\). Making use of equation (4.1), tabulation of the line-to-line voltage \((V_{ab})\) steps with their corresponding conduction angles is shown below.

<table>
<thead>
<tr>
<th>Voltage step (p.u)</th>
<th>Conduction angle (degrees)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2</td>
<td>0 to 29</td>
</tr>
<tr>
<td>-3</td>
<td>20 to 40</td>
</tr>
<tr>
<td>-3</td>
<td>40 to 60</td>
</tr>
<tr>
<td>-3</td>
<td>60 to 80</td>
</tr>
<tr>
<td>-2</td>
<td>80 to 100</td>
</tr>
</tbody>
</table>

**Table 4.3: line-to-line voltage (V_{ab}) steps of unmodulated 3-phase, 4-level inverter with their corresponding conduction angles.**
4.4: UNMODULATED 3-PHASE, 5-LEVEL INVERTER.

Shown in Fig. 3.9 is the space vector diagram of the switching state vectors of 3-phase, 5-level inverter. For an unmodulated condition, the coordinates of the outer hexagonal ring of this diagram form the switching state vectors of the 3-phase, 5-level inverter. Each voltage step has a conduction angle of \((360/24)° = 15°\). Thus, the line-to-line voltage \((V_{ab})\) steps with their corresponding conduction angles are tabulated under.

Table 4.4: Line-to-line voltage \((V_{ab})\) steps of unmodulated 3-phase, 5-level inverter with their corresponding conduction angles.

<table>
<thead>
<tr>
<th>Voltage step ((\mu_u))</th>
<th>Conduction angle (degrees)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-4</td>
<td>0 to 15</td>
</tr>
<tr>
<td>-4</td>
<td>15 to 30</td>
</tr>
<tr>
<td>-4</td>
<td>30 to 45</td>
</tr>
<tr>
<td>-4</td>
<td>45 to 60</td>
</tr>
<tr>
<td>-4</td>
<td>60 to 75</td>
</tr>
<tr>
<td>-3</td>
<td>75 to 90</td>
</tr>
<tr>
<td>-2</td>
<td>90 to 105</td>
</tr>
<tr>
<td>-1</td>
<td>105 to 120</td>
</tr>
<tr>
<td>0</td>
<td>120 to 135</td>
</tr>
<tr>
<td>1</td>
<td>135 to 150</td>
</tr>
<tr>
<td>2</td>
<td>150 to 165</td>
</tr>
<tr>
<td>3</td>
<td>165 to 180</td>
</tr>
</tbody>
</table>

100 to 120
120 to 140
140 to 160
160 to 180
180 to 200
200 to 220
220 to 240
240 to 260
260 to 280
280 to 300
300 to 320
320 to 340
340 to 360
From tables 4.1 through 4.4, plots of the line-to-line voltage \( (V_{in}) \) waveforms for the different levels of 3-phase, unmodulated inverters are presented as follows.

---

<table>
<thead>
<tr>
<th>Level</th>
<th>Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>180 to 195</td>
</tr>
<tr>
<td>4</td>
<td>195 to 210</td>
</tr>
<tr>
<td>4</td>
<td>210 to 225</td>
</tr>
<tr>
<td>4</td>
<td>225 to 240</td>
</tr>
<tr>
<td>4</td>
<td>240 to 255</td>
</tr>
<tr>
<td>3</td>
<td>255 to 270</td>
</tr>
<tr>
<td>2</td>
<td>270 to 285</td>
</tr>
<tr>
<td>1</td>
<td>285 to 300</td>
</tr>
<tr>
<td>0</td>
<td>300 to 315</td>
</tr>
<tr>
<td>-1</td>
<td>315 to 330</td>
</tr>
<tr>
<td>-2</td>
<td>330 to 345</td>
</tr>
<tr>
<td>-3</td>
<td>345 to 360</td>
</tr>
</tbody>
</table>

---

FIG. 4.1: VOLTAGE WAVEFORM OF UNMODULATED 3-PHASE 2-LEVEL INVERTER.
FIG. 4.1: VOLTAGE WAVEFORM OF UNMODULATED 3-PHASE, 3-LEVEL INVERTER.

FIG. 4.2: VOLTAGE WAVEFORM OF UNMODULATED 3-PHASE, 4-LEVEL INVERTER.
4.5: SPACE VECTOR MODULATED 3-PHASE, 3-LEVEL INVERTER WITH LINE-TO-LINE VOLTAGE ($V_{L-L}$) OF 1.8$V_{dc}$ AND SAMPLING ANGLE ($\omega_T$) OF 60°.

If $t_s$ is the sampling period of the reference voltage vector in a space vector modulation, moving at an angular velocity of $\omega_s$, then the sampling angle becomes $\omega_T$. Thus, the frequency modulation index is defined as

$$m_f = \frac{2\pi}{\omega_s t_s}, \text{ if } \omega_s \text{ is in radian,}$$
$$m_f = \frac{360}{\omega_s t_s}, \text{ if } \omega_s \text{ is in degrees.}$$

Also, if the amplitude of the line-to-line reference voltage vector is $V_{L-L}$, then the amplitude modulation index is defined as

$$m_a = \frac{V_{L-L}}{\left[(m-1)V_{dc}\right]}$$

To proceed with the modulation process, we need to know what the
reference voltage vector is, $V_{ref}$. A thoughtful and careful selection of the amplitude line-to-line voltage, $V_{L-L}$, and the sampling angle, $\omega_s T_s$, distinctly define $V_{ref}$ as could be seen from equation (3.10), i.e.,

$$
V_{ref} = V_{L-L} \begin{bmatrix}
\cos(\omega_t)

\cos(\omega_t - 2\pi/3)

\cos(\omega_t + 2\pi/3)
\end{bmatrix}
$$

Also, from equations (4.2) and (4.3), we could see that

$$
m_l = \frac{360}{\omega_s T_s}
$$

Then, we have

$$
m_l = \frac{360}{60} = 6
$$

So, from equations (4.2) and (4.3), we could see that

$$
m_n = \frac{V_{L-L}}{(m-1)V_{dc}}
$$

$$\
\Rightarrow m_n = \frac{1.8}{2} = 0.9
$$

Hence, these indicate that the modulation is within the linear range; and that the reference voltage vector has to be sampled 6 times within the switching cycle.

The computation proceeds as follows:

For $\omega_s T_s = 60^\circ$

$$
V_{ref} = 1.8V_{dc} \begin{bmatrix}
\cos(60)

\cos(60-120)

\cos(60+120)
\end{bmatrix}
$$

$$\
\Rightarrow V_{ref} = 1.8V_{dc} \begin{bmatrix} 0.5 \\
0.5 \\
-1 \end{bmatrix}
$$

Transforming to the two-dimensional coordinate plane,
\[ V_{\text{ref},gh} = 1.3V_{\text{pk}} \]
\[ V_{\text{ref},h} = 1 \quad 2 \quad 1 \quad 0.5 \quad 0.9 \]
\[ 3V_{\text{pk}} = 1 \quad 2 \quad 1 \quad 0.5 \quad 0.9 \]

i.e., \( V_{\text{ref},gh} = 0.9 \); \( V_{\text{ref},h} = 0.9 \).

With reference to Fig. 3.10, \( V_{\text{ref},gh} \) fall inside the parallelogram

As discussed earlier,

\[ V_{\text{UL}} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \quad V_{\text{UL}} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad V_{\text{IH}} = \begin{bmatrix} 1 \\ 1 \end{bmatrix}, \quad V_{\text{IL}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \]

But \( V_{\text{UL}} \) and \( V_{\text{IH}} \) are always the two nearest vectors, the third nearest vector is found by evaluating equation (3.18)

\[ V_{\text{ref}h} + V_{\text{ref}h} \ominus (V_{\text{UL},h} + V_{\text{UL},h}) \]

\[ \Rightarrow 0.9 + 0.9 - (1 + 0) = 0.8 \]

As it positive, \( V_{\text{UL}} \) becomes the third nearest vector.

The three nearest vectors are

\[ V_{\text{UL}} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \quad V_{\text{UL}} = \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \quad V_{\text{UL}} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \]

Their duty cycles are computed using equation (3.21)

\[ d_{\text{UL}} = (V_{\text{ref},h} \ominus V_{\text{UL},h}) \]
\[ d_{\text{UL}} = (V_{\text{ref},h} \ominus V_{\text{UL},h}) \]
\[ d_{\text{LL}} = 1 - d_{\text{UL}} - d_{\text{UL}} \]
\[ d_{UL} = (0.9 - 1) = 0.1 \]
\[ d_{LV} = (0.9 - 1) = 0.1 \]
\[ d_{LU} = 1 - 0.1 - 0.1 = 0.8 \]

Let, \[ u_L / u_c = \omega_{UL} / \omega_c = d_{UL} \]
\[ \Rightarrow \omega_{UL} = \omega_c \cdot d_{UL} = 60 \times 0.1 = 6^\circ \]
\[ \Rightarrow \omega_{LU} = \omega_c \cdot d_{LU} = 60 \times 0.1 = 6^\circ \]
\[ \Rightarrow \omega_{UV} = \omega_c \cdot d_{UV} = 60 \times 0.8 = 48^\circ \]

Transforming back to the three-dimensional coordinate plane using equation (3.22)

\[
\begin{bmatrix}
    k \\
    k - g \\
    k - g - h
\end{bmatrix}
\]

**k** should take values \([0, 1, \ldots, M-1]\), i.e., \([0, 1, 2]\), and

**there should be no negative sign in the mapped elements.**

Therefore,

\[ V_{UL} = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \]
\[ \Rightarrow \begin{bmatrix} 1 \\ 0 \end{bmatrix} \text{ and } \begin{bmatrix} 2 \\ 1 \end{bmatrix} \]

\[ V_{LU} = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \]
\[ \Rightarrow \begin{bmatrix} 1 \\ 0 \end{bmatrix} \text{ and } \begin{bmatrix} 2 \\ 1 \end{bmatrix} \]

\[ V_{UV} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \]
With reference to fig. 3.7, the positions of the above switching state vectors in the switching state vector diagram form the triangle shown below.

The sequences of switching are

221 → 211 → 210 → 110
221 → 211 → 210 → 110

For \( \omega_s t = 120' \)

\[
V_{ref} = 1.8V_{dc} \begin{bmatrix}
\cos(120)
\cos(120-120)
\cos(120+120)
\end{bmatrix}
\]

\[
\Rightarrow V_{ref} = 1.8V_{dc} \begin{bmatrix}
-0.5
1
-0.5
\end{bmatrix}
\]

Transforming to the two-dimensional coordinate plane,
\[
V_{ref, ph} = 1.8V_\alpha \
\begin{bmatrix}
2 & -1 & -1 \\
3V_\alpha & -1 & 2 & -1 & 1
\end{bmatrix} = \begin{bmatrix}
-0.9 \\
1.8 \\
-0.5
\end{bmatrix}
\]

i.e., \( V_{ref, ph} = -0.9 \), \( V_{ref, h} = -1.8 \).

In fig. 3.10, \( V_{ref, ph} \) fall inside the parallelogram.

That is
\[
V_{UL} = \begin{bmatrix}
0 \\
1
\end{bmatrix}, \quad V_{UL} = \begin{bmatrix}
-1 \\
2
\end{bmatrix}, \quad V_{UL} = \begin{bmatrix}
0 \\
2
\end{bmatrix}, \quad V_{UL} = \begin{bmatrix}
-1 \\
1
\end{bmatrix}.
\]

\[
V_{ref, ph} + V_{ref, h} * (V_{UL, ph} + V_{UL, h}) = (-0.9 + 1.8) - (0 + 1) = -0.1
\]

As it negative, \( V_{UL} \) becomes the third nearest vector.

The three nearest vectors are
\[
V_{UL} = \begin{bmatrix}
0 \\
1
\end{bmatrix}, \quad V_{UL} = \begin{bmatrix}
-1 \\
2
\end{bmatrix}, \quad V_{UL} = \begin{bmatrix}
-1 \\
1
\end{bmatrix}.
\]

Their duty cycles are computed using equation (3.20)
\[
d_{UL} = V_{ref, ph} - V_{UL, ph} \\
d_{UL} = V_{ref, h} - V_{UL, h} \\
d_{UL} = 1 - d_{UL} - d_{UL} \Rightarrow d_{UL} = 0.1 \\
d_{UL} = 1.8 - 1 = 0.8 \\
d_{UL} = 1 - 0.1 - 0.8 = 0.1
\]
Transforming back to the three-dimensional coordinate plane

\[ V_{1n} = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \]

\[ \Rightarrow \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix} \text{ and } \begin{bmatrix} 2 \\ 2 \\ 1 \end{bmatrix} \]

\[ V_{2n} = \begin{bmatrix} 1 \\ -1 \\ 2 \end{bmatrix} \]

\[ \Rightarrow \begin{bmatrix} 1 \\ 2 \\ 0 \end{bmatrix} \]

\[ V_{3n} = \begin{bmatrix} -1 \\ 0 \\ 1 \end{bmatrix} \]

\[ \Rightarrow \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} \text{ and } \begin{bmatrix} 1 \\ 2 \\ 1 \end{bmatrix} \]

In Fig. 3.7, these correspond to

120

B

<table>
<thead>
<tr>
<th>121</th>
<th>221</th>
</tr>
</thead>
<tbody>
<tr>
<td>010</td>
<td>110</td>
</tr>
</tbody>
</table>
The sequences of switching are
\[
\begin{align*}
221 &\rightarrow 121 \rightarrow 120 \rightarrow 110* \\
121 &\rightarrow 120 \rightarrow 110 \rightarrow 010
\end{align*}
\]

The asterisks sequence is chosen because in going from triangle A to B, it begins and ends with the same switching states, i.e., there is no extra switch transition.

For \(\omega_s t = 180^\circ\)
\[
V_{\text{ref}} = 1.8V_{dc} \begin{bmatrix}
\cos(180) \\
\cos(180 - 120) \\
\cos(180 + 120)
\end{bmatrix}
\]
\[
\Rightarrow V_{\text{ref}} = 1.8V_{dc} \begin{bmatrix}
-1 \\
0.5 \\
0.5
\end{bmatrix}
\]

Transforming to the two-dimensional coordinate plane,
\[
V_{\text{ref,g,h}} = 1.8V_k \begin{bmatrix}
2 & -1 & -1 & -1.8 \\
-1 & 2 & -1 & 0.5 \\
-1 & -1 & 0.5 & 0.9
\end{bmatrix}
\]
i.e., \(V_{\text{ref,g}} = -1.8; V_{\text{ref,h}} = 0.9\).
In fig. 3.10, \(V_{\text{ref,g,h}}\) fall inside the parallelogram.
That is

\[
V_{UL} = \begin{bmatrix} -1 \\ 0 \end{bmatrix}, \quad V_{LU} = \begin{bmatrix} -2 \\ 1 \end{bmatrix}, \quad V_{UL} = \begin{bmatrix} -1 \\ 1 \end{bmatrix}, \quad V_{LU} = \begin{bmatrix} -2 \\ 0 \end{bmatrix}.
\]

\[
V_{u|L} + V_{v|L} = (V_{UL} + V_{LU})
\]

\[
\Rightarrow (-1.8 + 0.9) - (-1 + 0) = 0.1
\]

As it positive, \( V_{u|L} \) becomes the third nearest vector.

The three nearest vectors are

\[
V_{UL} = \begin{bmatrix} -1 \\ 0 \end{bmatrix}, \quad V_{LU} = \begin{bmatrix} -2 \\ 1 \end{bmatrix}, \quad V_{UL} = \begin{bmatrix} -1 \\ 1 \end{bmatrix}, \quad V_{LU} = \begin{bmatrix} -2 \\ 0 \end{bmatrix}.
\]

Their duty cycles are computed using equation (3.20)

\[
\Rightarrow d_{UL} = - (0.9 - 1) = 0.1
\]

\[
\Rightarrow d_{LU} = - (-1.8 - 1) = 0.8
\]

\[
\Rightarrow d_{UL} = 1 - 0.1 = 0.8 = 0.1
\]

\[
\Rightarrow \omega_{UL} = \omega_{v} \times d_{UL} = 60 \times 0.1 = 6^\circ
\]

\[
\Rightarrow \omega_{LU} = \omega_{v} \times d_{LU} = 60 \times 0.8 = 48^\circ
\]

\[
\Rightarrow \omega_{UL} = \omega_{v} \times d_{UL} = 60 \times 0.1 = 6^\circ
\]

Transforming back to the three-dimensional coordinate plane

\[
V_{UL} = \begin{bmatrix} -1 \\ 0 \end{bmatrix}
\]
In fig. 3.7, these correspond to

$$V_{LU} = \begin{bmatrix} -2 \\ 1 \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} 0 \\ 2 \\ 1 \end{bmatrix}$$

$$V_{GU} = \begin{bmatrix} -1 \\ 1 \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} 0 \\ 1 \\ 2 \\ 1 \end{bmatrix}$$

021

\[122 \quad 011\]
\[011 \quad 010\]

The sequences of switching are

122 $\rightarrow$ 121 $\rightarrow$ 021 $\rightarrow$ 011

121 $\rightarrow$ 021 $\rightarrow$ 011 $\rightarrow$ 010

The asterisks sequence is chosen in going from triangle B to C.
For $\omega \Delta \theta = 240^\circ$

$$V_{\text{ref}} = 1.8V_{\text{d}} \begin{bmatrix} \cos(240) \\ \cos(240 + 120) \\ \cos(240 - 120) \end{bmatrix}$$

$$\Rightarrow V_{\text{ref}} = 1.8V_{r} \begin{bmatrix} -0.5 \\ -0.5 \\ 1 \end{bmatrix}$$

Transforming to the two-dimensional coordinate plane,

$$V_{\text{ref}, gh} = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 1 \end{bmatrix} V_{r} \begin{bmatrix} -0.5 \\ -0.5 \\ 1 \end{bmatrix} = \begin{bmatrix} -0.9 \\ -0.9 \end{bmatrix}$$

i.e., $V_{\text{ref}, gh} = -0.9; V_{\text{ref}, h} = -0.9$.

In fig. 3.10, $V_{\text{ref}, gh}$ fall inside the parallelogram

-1.0
0.0
upper, U

-1.0
-1.0
lower, L

That is

$$V_{\text{IL}} = \begin{bmatrix} 0 \\ -1 \end{bmatrix}, \quad V_{\text{LH}} = \begin{bmatrix} -1 \\ 0 \end{bmatrix}, \quad V_{\text{UL}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \quad V_{\text{IL}} = \begin{bmatrix} -1 \end{bmatrix}$$

$$V_{\text{ref}} + V_{\text{ref}, h} - (V_{\text{IL}} + V_{\text{IL}, h}) \Rightarrow (-2 \cdot 0.9) - (0 - 0) = -0.8$$

As it negative, $V_{\text{IL}}$ becomes the third nearest vector.
The three nearest vectors are
Their duty cycles are computed using equation (3.20)

\[ d_{1r} = 0.9 - 1 = 0.1 \]
\[ d_{1t} = 0.9 - 1 = 0.1 \]
\[ d_{1l} = 1 - 0.1 - 0.1 = 0.8 \]

\[ \omega_{t_{1r}} = \omega_{t_1} \cdot d_{1r} = 60 \cdot 0.1 = 6^\prime \]
\[ \omega_{t_{1t}} = \omega_{t_1} \cdot d_{1t} = 60 \cdot 0.1 = 6^\prime \]
\[ \omega_{t_{1l}} = \omega_{t_1} \cdot d_{1l} = 60 \cdot 0.8 = 48^\prime \]

Transforming back to the three-dimensional coordinate plane

\[ V_{1r} = \begin{bmatrix} 0 \\ -1 \end{bmatrix} \]
\[ \Rightarrow \begin{bmatrix} 0 \\ 1 \\ 1 \end{bmatrix} \text{ and } \begin{bmatrix} 0 \\ 1 \\ 2 \end{bmatrix} \]

\[ V_{1t} = \begin{bmatrix} -1 \\ 0 \end{bmatrix} \]
\[ \Rightarrow \begin{bmatrix} 1 \\ 1 \\ 2 \end{bmatrix} \]

\[ V_{1l} = \begin{bmatrix} -1 \\ -1 \end{bmatrix} \]
\[ \Rightarrow \begin{bmatrix} 0 \\ 1 \\ 2 \end{bmatrix} \]

In fig. 3.7, these correspond to
The sequences of switching are

122 → 112 → 021 → 012*

112 → 012 → 011 → 001

The asterisks sequence is chosen in going from triangle \( \triangle C \) to \( \triangle D \).

For \( \omega_{a,b} = 300^\circ \)

\[
V_{ref} = 1.8V_e \begin{bmatrix}
\cos(300)

\cos(300 - 120)

\cos(300 + 120)
\end{bmatrix}
\]

\[
= \begin{bmatrix}
0.5

-1

0.5
\end{bmatrix}
\]

Transforming to the two-dimensional coordinate plane,

\[
V_{ref,ab} = \begin{bmatrix}
2 & -1 & -1 & 0.5 & 0.9

1.8V_e & -1 & 2 & -1 & -1.8

V_e & 2 & -1 & -1 & -1.8

0.5 & -1 & 2 & -1 & -1.8
\end{bmatrix}
\]

i.e., \( V_{ref,b} = 0.9; V_{ref,b} = -1.8 \)

In fig. 3.10, \( V_{ref,ab} \) fall inside the parallelogram.
0.1

That is

\[ V_{UL} = \begin{bmatrix} 1 \\ -2 \end{bmatrix}, \quad V_{LU} = \begin{bmatrix} 0 \\ -1 \end{bmatrix}, \quad V_{UL} = \begin{bmatrix} 1 \\ -1 \end{bmatrix}, \quad V_{LU} = \begin{bmatrix} 0 \\ -2 \end{bmatrix}. \]

\[ V_{refX} + V_{refy} - (V_{UL} + V_{UL}) \rightarrow (0.9 - 1.8) - (1 - 2) = 0.3 \]

As it is positive, \( V_{UL} \) becomes the third nearest vector.

The three nearest vectors are

\[ V_{UL} = \begin{bmatrix} 1 \\ -2 \end{bmatrix}, \quad V_{LU} = \begin{bmatrix} 0 \\ -1 \end{bmatrix}, \quad V_{UL} = \begin{bmatrix} 1 \\ -1 \end{bmatrix}. \]

Their duty cycles are computed using equation (3.20)

\[ \Rightarrow d_{UL} = -(1.8 - 1) = 0.8 \]
\[ \Rightarrow d_{LU} = -(0.9 - 1) = 0.1 \]
\[ \Rightarrow d_{UL} = 1 \cdot 0.1 - 0.8 = 0.1 \]

\[ \Rightarrow \omega_{UL} = \omega_{LU} \cdot d_{UL} = 60 \cdot 0.8 = 48^\circ \]
\[ \Rightarrow \omega_{LU} = \omega_{LU} \cdot d_{LU} = 60 \cdot 0.1 = 6^\circ \]
\[ \Rightarrow \omega_{UL} = \omega_{LU} \cdot d_{UL} = 60 \cdot 0.1 = 6^\circ . \]

Transforming back to the three-dimensional coordinate plane

\[ V_{UL} = \begin{bmatrix} 1 \\ -2 \end{bmatrix} \]
The sequences of switching are

\[ 212 \rightarrow 112 \rightarrow 102 \rightarrow 101 \]

\[ 112 \rightarrow 102 \rightarrow 101 \rightarrow 001^* \]

The asterisks sequence is chosen in going from triangle D to E.

For \( \alpha_d = 360^\circ \)
Transforming to the two-dimensional coordinate plane,

\[
V_{\text{ref,}\perp} = \begin{bmatrix}
\cos(360) & \\
\cos(360 - 120) & \\
\cos(360 + 120) & \\
\end{bmatrix} \begin{bmatrix}
1.8V_\infty \\
0.5 \\
-0.5 \\
\end{bmatrix}
\]

\[
\Rightarrow V_{\text{ref}} = 1.8V_\infty
\]

In fig. 3.10, \(V_{\text{ref},h}\) fall inside the parallelogram that is negative, \(V_{\text{ref},v}\) becomes the third nearest vector.

The three nearest vectors are
Their duty cycles are computed using equation (3.20)

\[
\begin{align*}
\Rightarrow d_{UL} &= 1.8 - 1 = 0.8 \\
\Rightarrow d_{LU} &= -0.9 - (-1) = 0.1 \\
\Rightarrow d_{LL} &= 1 - 0.1 - 0.8 = 0.1 \\
\Rightarrow \omega_{UL} &= \omega_c \ast d_{UL} = 60 \ast 0.8 = 48^\circ \\
\Rightarrow \omega_{LU} &= \omega_c \ast d_{LU} = 60 \ast 0.1 = 6^\circ \\
\Rightarrow \omega_{LL} &= \omega_c \ast d_{LL} = 60 \ast 0.1 = 6^\circ.
\end{align*}
\]

Transforming back to the three-dimensional coordinate plane

\[
V_{UL} = \begin{bmatrix} 2 \\ 2 \\ -1 \end{bmatrix}
\Rightarrow \begin{bmatrix} 2 \\ 0 \\ 1 \end{bmatrix}
\]

\[
V_{LU} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}
\Rightarrow \begin{bmatrix} 1 \\ 0 \end{bmatrix} \text{ and } \begin{bmatrix} 2 \\ 1 \\ 1 \end{bmatrix}
\]

\[
V_{LL} = \begin{bmatrix} 1 \\ 1 \end{bmatrix}
\Rightarrow \begin{bmatrix} 1 \\ 0 \end{bmatrix} \text{ and } \begin{bmatrix} 2 \\ 1 \\ 2 \end{bmatrix}
\]

In fig. 3.7, these correspond to
The sequences of switching are

\[ 212 \rightarrow 211 \rightarrow 201 \rightarrow 101^* \]
\[ 211 \rightarrow 201 \rightarrow 101 \rightarrow 100 \]

The asterisks sequence is chosen in going from triangle E to F.

The switching pattern for a cycle is

\[ 211 \rightarrow 210 \rightarrow 110 \rightarrow 100 \]
\[ 221 \rightarrow 121 \rightarrow 120 \rightarrow 110 \]
\[ 121 \rightarrow 021 \rightarrow 011 \rightarrow 010 \]
\[ 122 \rightarrow 012 \rightarrow 011 \]
\[ 112 \rightarrow 102 \rightarrow 101 \rightarrow 001 \]
\[ 212 \rightarrow 211 \rightarrow 201 \rightarrow 101 \]

At this juncture, application of equation (4.1) results in normalized, line-to-line voltage switching state vector sequences; with their respective conduction angles as superscripts. These sequences are shown below.
4.6: SPACE VECTOR MODULATED 3-PHASE, 3-LEVEL
INVERTER WITH LINE-TO-LINE VOLTAGE \( (V_{\text{L1L2}}) \) OF 1.8\( V_{\text{dc}} \)
AND SAMPLING ANGLE \( (\alpha_T) \) OF 30°.

For this modulation condition, equations (4.2) and (4.3) give the
modulation parameters as

\[
m_t = \frac{360}{\omega_0 T_s}
\]

\[
\Rightarrow m_t = \frac{360}{30} = 12
\]

\[
m_s = \frac{V_{\text{L1L2}}}{\left| (m-1) V_{\text{dc}} \right|}
\]

\[
\Rightarrow m_s = \frac{1.8}{2} = 0.9
\]

This implies that the reference voltage vector has to be sampled 12 times
within the switching cycle.

As already typified in subchapter 4.5, the same computational steps are
involved. Therefore, the switching pattern for a cycle is

\[
\begin{align*}
211 &\rightarrow 210 \rightarrow 200 \rightarrow 100 \\
211 &\rightarrow 210 \rightarrow 110 \rightarrow 100 \\
221 &\rightarrow 220 \rightarrow 210 \rightarrow 110 \\
221 &\rightarrow 121 \rightarrow 120 \rightarrow 110
\end{align*}
\]
The normalized, line-to-line voltage switching state vector sequences, with their respective conduction angles as superscripts are:

\[
\begin{align*}
[1 \ 0 \ 1]^{3.3} &\rightarrow [1 \ 1 \ -2]^9 \rightarrow [2 \ 0 \ -2]^{8.4} \rightarrow [1 \ 0 \ -1]^{3.3} \\
[1 \ 0 \ -1]^{8.75} &\rightarrow [1 \ 1 \ -2]^{12} \rightarrow [0 \ 1 \ -1]^{1.5} \rightarrow [1 \ 0 \ -1]^{0.75} \\
[0 \ 1 \ -1]^{3.3} &\rightarrow [0 \ 2 \ -2]^{8.4} \rightarrow [1 \ 1 \ -2]^8 \rightarrow [0 \ 1 \ -1]^{3.3} \\
[0 \ 1 \ -1]^{8.75} &\rightarrow [-1 \ 1 \ 0]^{1.5} \rightarrow [-1 \ 2 \ -1]^{12} \rightarrow [0 \ 1 \ -1]^{0.75} \\
[-1 \ 1 \ 0]^{3.3} &\rightarrow [-2 \ 1 \ 1]^9 \rightarrow [-2 \ 2 \ 0]^{8.4} \rightarrow [-1 \ 1 \ 0]^{3.3} \\
[-1 \ 1 \ 0]^{8.75} &\rightarrow [-2 \ 1 \ 1]^{12} \rightarrow [-1 \ 0 \ 1]^{1.5} \rightarrow [-1 \ 0 \ 0]^{0.75} \\
[-1 \ 0 \ 1]^{3.3} &\rightarrow [-2 \ 0 \ 1]^{8.4} \rightarrow [-2 \ 1 \ 1]^9 \rightarrow [-1 \ 0 \ 1]^{3.3} \\
[-1 \ 0 \ 1]^{8.75} &\rightarrow [0 \ -1 \ 1]^{1.5} \rightarrow [-1 \ -2]^{12} \rightarrow [-1 \ 0 \ 1]^{0.75} \\
[0 \ -1 \ 1]^{3.3} &\rightarrow [-1 \ -2]^9 \rightarrow [0 \ -2 \ 2]^{8.4} \rightarrow [0 \ -1 \ 1]^{3.3} \\
[0 \ -1 \ 1]^{8.75} &\rightarrow [1 \ -2 \ 1]^{12} \rightarrow [1 \ -1 \ 0]^{1.5} \rightarrow [1 \ -1 \ 0]^{0.75} \\
[1 \ -1 \ 0]^{3.3} &\rightarrow [2 \ -2 \ 0]^{8.3} \rightarrow [2 \ -1 \ -1]^9 \rightarrow [1 \ -1 \ 0]^{3.3}
\end{align*}
\]
4.7: SPACE VECTOR MODULATED 3-PHASE, 3-LEVEL INVERTER WITH LINE-TO-LINE VOLTAGE \( V_{L-L} \) OF \( 1.8V_{dc} \) AND SAMPLING ANGLE \( (\omega, T_s) \) OF 20°.

In this very case, the modulation parameters are given as

\[
m_r = 360/\omega T_s
\]

\[
\Rightarrow m_r = 360/20 = 18.
\]

\[
m_a = V_{L-L}/[(m-1)V_{dc}]
\]

\[
\Rightarrow m_a = 1.8/2 = 0.9
\]

Hence, the reference voltage vector has to be sampled 18 times within the switching cycle.

The switching pattern for a cycle, following the same computational steps as above, is

\[
211 \rightarrow 201 \rightarrow 200 \rightarrow 100
\]
\[
211 \rightarrow 210 \rightarrow 200 \rightarrow 100
\]
\[
211 \rightarrow 210 \rightarrow 110 \rightarrow 190
\]
\[
221 \rightarrow 220 \rightarrow 210 \rightarrow 110
\]
\[
221 \rightarrow 220 \rightarrow 120 \rightarrow 110
\]
\[
221 \rightarrow 121 \rightarrow 120 \rightarrow 110
\]
\[
121 \rightarrow 120 \rightarrow 020 \rightarrow 010
\]
\[
121 \rightarrow 021 \rightarrow 020 \rightarrow 010
\]
\[
121 \rightarrow 021 \rightarrow 011 \rightarrow 010
\]
The normalized, line-to-line voltage switching state vector sequences, with their respective conduction angles as superscripts are:

\[
\begin{align*}
[1 & 0 -1]^{1.55} \rightarrow [2 -1 -1]^{1.1} \rightarrow [2 0 -2]^{1.8} \rightarrow [1 0 -1]^{1.55} \\
[1 & 0 -1]^{1.55} \rightarrow [1 1 -2]^{2.4} \rightarrow [2 0 -2]^{1.8} \rightarrow [1 0 -1]^{1.55} \\
[0 & 1 -1]^{0.3} \rightarrow [1 1 -2]^{0.8} \rightarrow [0 1 -1]^{1.1} \rightarrow [1 0 -1]^{0.5} \\
[0 & 1 -1]^{1.55} \rightarrow [0 2 -2]^{3.8} \rightarrow [1 1 -2]^{1.1} \rightarrow [0 1 -1]^{1.55} \\
[0 & 1 -1]^{1.55} \rightarrow [0 2 -2]^{3.8} \rightarrow [-1 2 -1]^{1.1} \rightarrow [0 1 -1]^{1.55} \\
[0 & 1 -1]^{0.3} \rightarrow [-1 1 0]^{1.1} \rightarrow [-1 2 -1]^{0.8} \rightarrow [0 1 -1]^{0.5} \\
[-1 & 1 0]^{1.55} \rightarrow [-1 2 -1]^{1.1} \rightarrow [-2 2 0]^{1.3} \rightarrow [-1 1 0]^{1.55} \\
[-1 & 1 0]^{1.55} \rightarrow [-2 1 1]^{1.1} \rightarrow [-2 2 0]^{1.3} \rightarrow [-1 1 0]^{1.55} \\
[-1 & 1 0]^{0.5} \rightarrow [-2 1 1]^{1.1} \rightarrow [-1 0 1]^{1.1} \rightarrow [-1 1 0]^{0.5} \\
[-1 & 0 1]^{1.55} \rightarrow [-2 0 2]^{3.8} \rightarrow [-2 1 1]^{3.1} \rightarrow [-1 0 1]^{1.55}
\end{align*}
\]
\[
[-1 \\ 0 \\ 1]^T^{0.5} \rightarrow [0 \\ -1 \\ 0]^T \quad \rightarrow [-1 \\ -1 \\ -2]^T \quad \rightarrow [-1 \\ 1 \\ -2]^T^{3.5} \\
[-1 \\ 0 \\ 1]^T^{0.5} \rightarrow [0 \\ -1 \\ 1]^T \quad \rightarrow [0 \\ -1 \\ 2]^T^{3.5} \\
[0 \\ -1 \\ 1]^T^{1.5} \rightarrow [-1 \\ -2 \\ -2]^T \quad \rightarrow [0 \\ -1 \\ 2]^T^{3.5} \\
[0 \\ -1 \\ 1]^T^{1.5} \rightarrow [1 \\ -2 \\ 1]^T \quad \rightarrow [0 \\ -1 \\ 2]^T^{3.5} \\
[0 \\ -1 \\ 1]^T^{0.5} \rightarrow [1 \\ -2 \\ 2]^T \quad \rightarrow [1 \\ -1 \\ 0]^T^{1.5} \\
[0 \\ -1 \\ 1]^T^{0.5} \rightarrow [2 \\ -2 \\ 2]^T \quad \rightarrow [1 \\ -1 \\ 0]^T^{1.5} \\
[1 \\ 1 \\ 0]^T^{3.5} \rightarrow [2 \\ -2 \\ 2]^T^{3.8} \\
[1 \\ 1 \\ 0]^T^{1.5} \rightarrow [2 \\ -2 \\ 1]^T^{3.1} \\
[1 \\ 0 \\ 0]^T^{0.5} \rightarrow [1 \\ -1 \\ 1]^T \quad \rightarrow [1 \\ -1 \\ 0]^T^{0.5} \\
[1 \\ 0 \\ 0]^T^{0.5} \rightarrow [2 \\ -1 \\ 1]^T \quad \rightarrow [1 \\ -1 \\ 0]^T^{0.5} \\
[1 \\ 0 \\ 0]^T^{0.5} \rightarrow [2 \\ -1 \\ 0]^T \quad \rightarrow [1 \\ -1 \\ 0]^T^{0.5} \\
[1 \\ 0 \\ 0]^T^{0.5} \rightarrow [1 \\ -0 \\ -1]^T \\
[1 \\ 0 \\ 0]^T^{0.5} \rightarrow [2 \\ -0 \\ -1]^T \\
[1 \\ 0 \\ 0]^T^{0.5} \rightarrow [1 \\ 0 \\ -1]^T.
\]

4.3: SPACE VECTOR MODULATED 3-PHASE, 3-LEVEL INVERTER WITH LINE-TO-LINE VOLTAGE (V_{L-L}) OF 1.8\sqrt{3}V_{dc} AND SAMPLING ANGLE (\omega_sT) OF 30°.

The frequency and amplitude modulation indices are given as:

\[
m_t = 360 / \omega_s T.
\]

\[
\Rightarrow m_t = 360 / 10 = 36.
\]

\[
m_a = V_{L-L} / \{ (m-1)V_{dc} \}
\]

\[
\Rightarrow m_a = 1.8 / 2 = 0.9
\]

Thirty-six (36) sampling rate is employed within the switching cycle. The switching pattern for a cycle, following the same computational steps as above, is:

- 211 → 201 → 200 → 106
- 211 → 201 → 200 → 100
- 211 → 201 → 200 → 100
211 → 210 → 200 → 100
211 → 210 → 200 → 100
211 → 210 → 110 → 100
221 → 220 → 210 → 110
221 → 220 → 210 → 110
221 → 220 → 210 → 110
221 → 220 → 120 → 110
221 → 220 → 120 → 110
221 → 121 → 120 → 110
121 → 120 → 020 → 010
121 → 120 → 020 → 010
121 → 120 → 020 → 010
121 → 021 → 020 → 010
121 → 021 → 020 → 010
121 → 021 → 011 → 010
122 → 022 → 021 → 011
122 → 022 → 021 → 011
122 → 022 → 021 → 011
122 → 020 → 012 → 011
122 → 022 → 012 → 011
The normalized, line-to-line voltage switching state vector sequences; with their respective conduction angles as superscripts are

\[
\begin{align*}
122 & \rightarrow 112 \rightarrow 012 \rightarrow 011 \\
112 & \rightarrow 012 \rightarrow 002 \rightarrow 001 \\
112 & \rightarrow 012 \rightarrow 002 \rightarrow 001 \\
112 & \rightarrow 102 \rightarrow 002 \rightarrow 001 \\
112 & \rightarrow 102 \rightarrow 002 \rightarrow 001 \\
112 & \rightarrow 102 \rightarrow 101 \rightarrow 001 \\
212 & \rightarrow 202 \rightarrow 102 \rightarrow 101 \\
212 & \rightarrow 202 \rightarrow 102 \rightarrow 101 \\
212 & \rightarrow 202 \rightarrow 102 \rightarrow 101 \\
212 & \rightarrow 202 \rightarrow 201 \rightarrow 101 \\
212 & \rightarrow 202 \rightarrow 201 \rightarrow 101 \\
212 & \rightarrow 211 \rightarrow 201 \rightarrow 101 \\
\end{align*}
\]

\[
\begin{align*}
[10 \! - \! 1]^0.775 & \rightarrow [2 \! - \! 1 \! - \! 1]^{3.1} \rightarrow [20 \! - \! 2]^{0.875} \rightarrow [10 \! - \! 1]^{0.575} \\
[10 \! - \! 1]^0.775 & \rightarrow [2 \! - \! 1 \! - \! 1]^{1.55} \rightarrow [20 \! - \! 2]^{1.9} \rightarrow [10 \! - \! 1]^{0.775} \\
[10 \! - \! 1]^{3.1} & \rightarrow [2 \! - \! 1 \! - \! 1]^{0} \rightarrow [20 \! - \! 2]^{2.8} \rightarrow [10 \! - \! 1]^{1.8} \\
[10 \! - \! 1]^0.775 & \rightarrow [11 \! - \! 2]^{1.55} \rightarrow [20 \! - \! 2]^{1.9} \rightarrow [10 \! - \! 1]^{0.775} \\
[10 \! - \! 1]^{0.55} & \rightarrow [11 \! - \! 2]^{3.1} \rightarrow [20 \! - \! 2]^{0.8} \rightarrow [10 \! - \! 1]^{0.85} \\
[10 \! - \! 1]^{0.25} & \rightarrow [11 \! - \! 2]^{4} \rightarrow [20 \! - \! 2]^{0.5} \rightarrow [10 \! - \! 1]^{0.25} \\
\end{align*}
\]
\begin{align*}
[0 \ 1 \ -1]^{0.55} & \rightarrow [0 \ 2 \ -2]^{0.8} \rightarrow [1 \ 1 \ -2]^{1.1} \rightarrow [0 \ 1 \ -1]^{0.55} \\
[0 \ 1 \ -1]^{0.775} & \rightarrow [0 \ 2 \ -2]^{1.9} \rightarrow [1 \ 1 \ -2]^{1.55} \rightarrow [0 \ 1 \ -1]^{0.775} \\
[0 \ 1 \ -1]^{1.1} & \rightarrow [0 \ 2 \ -2]^{2.8} \rightarrow [1 \ 1 \ -2]^{9} \rightarrow [0 \ 1 \ -1]^{1.1} \\
[0 \ 1 \ -1]^{0.575} & \rightarrow [0 \ 2 \ -2]^{1.9} \rightarrow [-1 \ 2 \ -1]^{1.55} \rightarrow [0 \ 1 \ -1]^{0.775} \\
[0 \ 1 \ -1]^{0.75} & \rightarrow [0 \ 2 \ -2]^{0.75} \rightarrow [-1 \ 2 \ -1]^{1.1} \rightarrow [0 \ 1 \ -1]^{0.575} \\
[0 \ 1 \ -1]^{0.25} & \rightarrow [0 \ 2 \ -2]^{0.5} \rightarrow [-1 \ 2 \ -1]^{4} \rightarrow [0 \ 1 \ -1]^{0.25} \\
[-1 \ 1 \ 0]^{0.75} & \rightarrow [-1 \ 2 \ -1]^{3.05} \rightarrow [-2 \ 2 \ 0]^{0.8} \rightarrow [-1 \ 1 \ 0]^{0.575} \\
[-1 \ 1 \ 0]^{0.25} & \rightarrow [-1 \ 2 \ -1]^{1.55} \rightarrow [-2 \ 2 \ 0]^{1.9} \rightarrow [-1 \ 1 \ 0]^{0.775} \\
[-1 \ 1 \ 0]^{1.1} & \rightarrow [-1 \ 2 \ -1]^{0} \rightarrow [-2 \ 2 \ 0]^{2.8} \rightarrow [-1 \ 1 \ 0]^{1.1} \\
[-1 \ 1 \ 0]^{0.775} & \rightarrow [-2 \ 1 \ 1]^{1.55} \rightarrow [-2 \ 2 \ 0]^{1.9} \rightarrow [-1 \ 1 \ 0]^{1.1} \\
[-1 \ 1 \ 0]^{0.75} & \rightarrow [-2 \ 1 \ 1]^{3.05} \rightarrow [-2 \ 2 \ 0]^{0.8} \rightarrow [-1 \ 1 \ 0]^{0.575} \\
[-1 \ 1 \ 0]^{0.25} & \rightarrow [-2 \ 1 \ 1]^{4} \rightarrow [-2 \ 2 \ 0]^{0.5} \rightarrow [-1 \ 1 \ 0]^{0.25} \\
[-1 \ 0 \ 1]^{0.75} & \rightarrow [-2 \ 0 \ 2]^{0.75} \rightarrow [-2 \ 1 \ 1]^{0.1} \rightarrow [-1 \ 1 \ 0]^{0.575} \\
[-1 \ 0 \ 1]^{0.75} & \rightarrow [-2 \ 0 \ 2]^{1.9} \rightarrow [-2 \ 1 \ 1]^{1.55} \rightarrow [-1 \ 1 \ 0]^{0.775} \\
[-1 \ 0 \ 1]^{1.1} & \rightarrow [-2 \ 0 \ 2]^{2.8} \rightarrow [-2 \ 1 \ 1]^{6} \rightarrow [-1 \ 1 \ 0]^{1.1} \\
[-1 \ 0 \ 1]^{0.25} & \rightarrow [-2 \ 0 \ 2]^{0.5} \rightarrow [-1 \ -1 \ 2]^{4} \rightarrow [-1 \ 1 \ 0]^{0.25} \\
[0 \ -1 \ 1]^{0.55} & \rightarrow [-1 \ -1 \ 2]^{1.55} \rightarrow [0 \ -2 \ 2]^{0.8} \rightarrow n[0 \ -1 \ 1]^{0.55} \\
[0 \ -1 \ 1]^{0.775} & \rightarrow [-1 \ -1 \ 2]^{1.55} \rightarrow [0 \ -2 \ 2]^{1.9} \rightarrow [0 \ -1 \ 1]^{0.775}
\end{align*}
Having realized the switching state sequences with their respective duty cycles for the sampled cases of three-phase, three-level inverter, arbitrarily choosing the sequences of modulation with parameters $\theta_{0} = 0^\circ$, $V_{L} = 1.8V_{dc}$, the per unit line-to-line voltage waveforms are shown in fig.4.5.

4.8: SPECIFIC HARMONIC ELIMINATION.

For a stepped waveform such as the one depicted in fig.2.13, the Fourier transform for this waveform is as follows

$$V(\omega t) = 4V_{dc}/\pi \sum_{n} \left[ \cos(n\theta_{1}) + \cos(n\theta_{2}) + \ldots + \cos(n\theta_{N}) \right] * \sin(\omega t) ------(4.4)$$

Where $n = 1, 3, 5, 7, \ldots$.

The magnitudes of the Fourier coefficients when normalized with respect to $V_{dc}$ are as follows
\[ H(n) = \frac{4}{\pi} \sum_{k=1}^{n} \left[ \cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_9) \right] \sin(\omega t) \]  \hspace{1cm} (4.5)

Where \( n = 1, 3, 5, 7, \ldots \).

The conducting angles \( \theta_1, \theta_2, \theta_3, \theta_4 \) can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [4]. For this 9-level inverter, the 5th, 7th, and 11th harmonics can be eliminated with the appropriate choice of the conduction angles. One degree of freedom is used so that the magnitude of the output waveform corresponds to the reference amplitude modulation index, \( m_a \), which is defined as

\[ V_{l,m} = \frac{V_{l,m}}{V_{l,ref}} \]

Where \( V_{l,m} \) is the amplitude command of the inverter output phase voltage, and \( V_{l,ref} \) is the maximum attainable amplitude of the inverter [2] given by

\[ V_{l,ref} = S \times V_{dc} \]  \hspace{1cm} (4.6)

Equations develop from equation (4.5) are as follows.

\[ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \]
\[ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \]
\[ \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) = 0 \]
\[ \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = m_a S \]  \hspace{1cm} (4.6)

Arbitrarily choosing \( m_a = 0.8 \), and \( S = 5 \) (i.e., from \( M = 2S + 1 \), where \( M = 9 \)), the set of nonlinear transcendental equations (4.6) is solved for conduction angles using MATLAB environment, [16]; the results are

\( \theta_1 = 9.8472^\circ \)
\( \theta_2 = 20.4794^\circ \)
\( \theta_3 = 38.5469^\circ \)
\( \theta_4 = 60.4993^\circ \)

This means that if the inverter output is symmetrically switched during the positive half cycle of the fundamental voltage to \( +V_{dc} \) at 9.8472°, +2\( V_{dc} \) at 20.4794°, +3\( V_{dc} \) at 38.5469°, +4\( V_{dc} \) at 60.4993°, and similarly in the negative half cycle to -\( V_{dc} \) at 189.8472°, -2\( V_{dc} \) at 200.4794°, -3\( V_{dc} \) at 218.5469°, -4\( V_{dc} \) at 240.4993°, the output voltage of the 9-level inverter will not contain the 5th, 7th, and 11th harmonic components.
FIG 4.6: LINE-TO-LINE VOLTAGE WAVEFORMS OF THREE-PHASE, THREE-LEVEL SPACE VECTOR MODULATED INVERTER: \( \omega_s = 60, V_{L-L} = 1.8 \text{Vdc} \).
CHAPTER FIVE.

HARMONIC EVALUATION AND FREQUENCY SPECTRA.

With reference to figures 3.1, 3.2, 3.3, 3.4, for the multi-carrier 5-level modulation; figures 4.1, 4.2, 4.3, 4.4, for the 2-, 3-, 4-, 5-level unmodulated space vector switching sequences; figure 4.5 for the modulated 3-level inverter; and also to the 3-level modulated inverter switching sequences, with their respective conduction angles, in subchapters 4.6, 4.7, 4.8; verification of the harmonic contents of each respective case accesses their performances.

Hence, evaluation of the Fourier coefficients \(a_n\) and \(b_n\) and the corresponding harmonic amplitudes \(C_n\) were carried out using the following equations [17]:

\[
a_n = \frac{1}{n \pi} \int_0^{2\pi} A \cos(n \theta) \, d\theta \quad (5.1)
\]

\[
b_n = \frac{1}{n \pi} \int_0^{2\pi} A \sin(n \theta) \, d\theta \quad (5.2)
\]

\[
C_n = \sqrt{(a_n)^2 + (b_n)^2} \quad (5.3)
\]

Where \(A\) is the per unit value of the voltage level.

Values of the harmonic amplitudes, \(C_n\), obtained for each of the above stated cases were plotted against the harmonic order, \(n\); resulting in the harmonic spectra display as shown below.
**FIG. 5.1:** HARMONIC SPECTRUM FOR APOD
\( m = 0.8, m_f = 20, M = 5 \)

**FIG. 5.2:** HARMONIC SPECTRUM FOR PD
\( m = 0.8, m_f = 20, M = 5 \)
FIG. 5.3: HARMONIC SPECTRUM FOR PCD  
\[ m = 0.0, \text{mf} = 20, M = 5 \]

FIG. 5.4: HARMONIC SPECTRUM FOR PS  
\[ m = 0.8, \text{mf} = 30, M = 5 \]
Figure 5.5: Harmonic Spectrum of Unmodulated 3-Phase 2-Level Inverter

Figure 5.6: Harmonic Spectrum of Unmodulated 3-Phase 3-Level Inverter
FIG. 5.9 HARMONIC SPECTRUM OF MODULATED 3-PHASE, 3-LEVEL INVERTER

\[ V_{dL} = 1.8 \text{Vdc}, \omega_T = 30, \text{i.e., sampling rate of 12.} \]

FIG. 5.10 HARMONIC SPECTRUM OF MODULATED 3-PHASE, 3-LEVEL INVERTER

\[ V_{dL} = 1.8 \text{Vdc}, \omega_T = 30, \text{i.e., sampling rate of 12.} \]
FIG 5.11: HARMONIC SPECTRUM OF MODULATED 3-PHASE, 3-LEVEL INVERTER
\( V_{dc} = 1.8\text{Vdc}, \omega t = 20, \text{i.e., sampling rate of } 10 \)

![Harmonic Spectrum](image)

FIG 5.12: HARMONIC SPECTRUM OF MODULATED 3-PHASE, 3-LEVEL INVERTER
\( V_{dc} = 1.8\text{Vdc}, \omega t = 10, \text{i.e., sampling rate of } 30 \)

![Harmonic Spectrum](image)
Having realized the harmonic spectra, it is quite imperative to make some deductions from them; as each spectrum truly unveils the operational performance level of the corresponding pulsewidth modulation scheme involved.

For the multi-carrier modulation technique applied to a 5-level voltage source inverter, the spectra of these schemes show that almost all harmonics are present; though at varying degree from one type to another. However, the phase disposition, PD, multi-carrier technique synthesized the highest amplitude of the per unit output fundamental voltage at the same modulation level with other type.

With reference to figures 5.5, 5.6, 5.7, and 5.8, it can be easily seen that the unmodulated, three-phase, 2-, 3-, 4-, and 5-level inverters have their respective harmonic orders, with the highest amplitude, as 5, 11, 17, and 23. In other words, a generalized series can be formed whose terms comprise of the harmonic order with the highest amplitude of an unmodulated, three-phase inverter, that is

\[ \text{HARMONIC ORDER WITH THE HIGHEST AMPLITUDE FOR M-LEVEL INVERTER} = 6M \]  

Where \( M \) is the inverter level.

Besides, the amplitude of the synthesized per unit fundamental output voltage of the inverter increases as the inverter level, \( M \), increases.

Figure 5.9 through 5.12 show the spectra of the space vector modulated three-phase, three-level inverter. For \( M \)-level space vector modulated inverter sampled at an angular distance, \( \omega_t \), the sampling rate per switching cycle is

\[ R = \frac{360}{\omega_t} \]  

Considering these spectra, it can then be generalized that the harmonic order nearest to the fundamental is \( R - 1 \).
CHAPTER SIX.

DISCUSSIONS AND CONCLUSIONS.

In this work, multilevel inverter types needed in high power applications such as utility and large motor drive applications, have been described and their control strategies given as carrier-based PWM, Specific Elimination PWM, and Space Vector PWM. It has been identified that the cascade multilevel inverter configuration with its preferred Specific Elimination PWM control has the attraction of not requiring extra circuit for voltage balancing; least number of circuit component and modularized nature of circuit layout. But its feature of multi-input dc supply is a limitation. The single stage multilevel inverter has the advantage of only one dc input with voltage levels defined by a capacitor bank.

The control of this single stage multilevel inverter has received considerable research attention. However, the harmonic profile and a generalized method of representing the possible output states of these inverters have so far received negligible attention.

In this work, a generalized truth-table for the switching states of multilevel inverters has been formulated. The formulation gives all possible states of an inverter output phase during switching action. Illustrations were given for different inverter levels and phases. The truth-table, inevitably will be applied to know exactly the dc input voltage level at which each active device in each phase of the multilevel inverter can be switched to, for a desired output voltage waveform.

Of all the single stage multilevel inverters, the Space Vector controlled type has received the most research attention because of its flexibility and high performance characteristics. This Space Vector controlled single stage inverter has therefore been given detailed attention in this work. The computational steps involved in the Space Vector Pulse Width Modulation process of multilevel voltage source inverters have been presented in detail. These computational steps remain the same regardless of the number of levels of the inverter. For minimum switching loss, the computational steps have been used to determine from the switching state vector diagram the optimum switching sequences for any given multilevel inverter. For three-level, three-phase multilevel inverter, a generalized pattern of the harmonic profile of the inverter output voltage waveforms under optimum switching operation for varying sampling periods has been determined using Fourier analysis. The Space Vector Pulse Width Modulated inverter, sampled at an
angular distance \( \omega t_s \), where \( t_s \) is the sampling time, has the sampling frequency ratio, \( R \), given as \( R = \frac{360}{\pi} \omega t_s \). It has been shown that the harmonic order nearest to the fundamental is the \((R-1)\)th harmonic order. This finding implies that harmonics equal to, or lower than the \((R-1)\)th harmonic order can be eliminated by choosing the appropriate sampling frequency ratio, \( R \).
REFERENCES.


